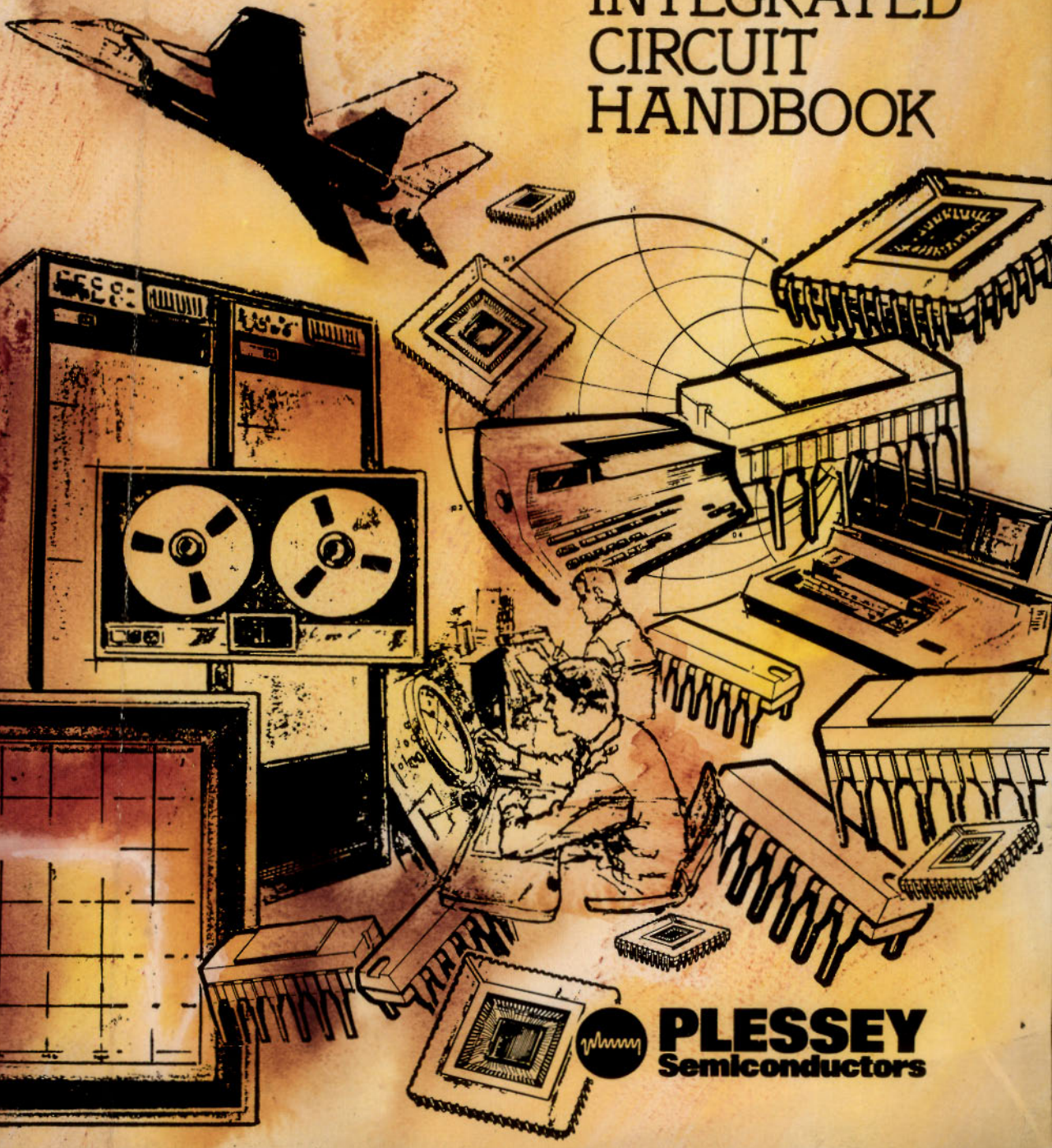
SP8000 SERIES
HIGH SPEED DIVIDERS
INTEGRATED CIRCUIT HANDBOOK



PLESSEY
Semiconductors

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SP8000 series high speed dividers

Plessey Semiconductors' SP8000 series leads the world in technical performance. One of the most comprehensive ranges of dividers available, the SP8000 series has been developed and extended to cater for the exacting requirements of the instrumentation and communications markets. The range includes prescalers from divide-by-2 up to divide-by-129, operating from 1Hz to 2.4GHz.

Suffix A Military	-55° C to +125° C
Suffix M Intermediate	-40° C to +85° C
Suffix B Commercial	-30° C to +70° C
	(0° C to +70° C in some cases)

Fixed modulus prescalers

Divide by	Type	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)			Max current (mA)	Output		Package		
		-55 +125	-40 +85	-30 +70	0 +70		5.0	5.2	6.8		TTL	ECL	Metal can	Ceramic	Plastic
2	SP8604A	●				300		●		18		●	●		
	SP8604B			●		300		●		18		●	●		
	SP8602A	●				500		●		18		●	●		
	SP8602B			●		500		●		18		●	●		
	SP8607A	●				600		●		18		●	●		
	SP8607B			●		600		●		18		●	●		
	SP8605A	●				1000		●		100		●		●	
	SP8605B				●	1000		●		100		●		●	
	SP8606A	●				1300		●		100		●		●	
	SP8606B				●	1300		●		100		●		●	
4	SP8790A	●				60	●			11	●		●		
	SP8790B			●		60	●			11	●		●		
	SP8601A	●				150		●		25	●	●	●		
	SP8601B			●		150		●		25	●	●	●		
	SP8600A	●				250		●		25	●	●	●		
	SP8600B			●		250		●		25	●	●	●		
	SP8610A	●				1000		●		100		●		●	
	SP8610B				●	1000		●		100		●		●	
	SP8611A	●				1300		●		100		●		●	
	SP8611B				●	1500		●		100		●		●	
	SP8612B				●	1800			●	110		●		●	
	SP8712B				●	2400			●	100		●		●	

Fixed modulus prescalers (continued)

5	SP8620A	●				400		●		55		●		●	
	SP8620B			●		400		●		55		●		●	
8	SP8794A	●				120	●			11	●		●		
	SP8794B			●		120	●			11	●		●		
	SP8670A	●				600		●		45		●		●	
	SP8670B			●		600		●		45		●		●	
	SP8735B				●	600		●		90	Ⓑ	●		●	
	SP8675B				●	1000			●	95		●		●	
	SP8678B				●	1500			●	95		●		●	
	SP8678M		●			1500			●	95		●		●	
10	SP8660A	●				150	●			13	●		●		
	SP8660B			●		150	●			13	●		●		
	SP8660			●		150	●			13	●				●
	SP8637B				●	400		●		90	Ⓑ	●		●	
	SP8630A	●				600		●		70		●		●	
	SP8630B			●		600		●		70		●		●	
	SP8635B				●	600		●		90	Ⓑ	●		●	
	SP8634B				●	700		●		90	Ⓑ	●		●	
	SP8665B				●	1000			●	105		●		●	
	SP8668B				●	1500			●	105		●		●	
16	SP8659A	●				200	●			13	●		●		
	SP8659B			●		200	●			13	●		●		
	SP8650A	●				600		●		45		●		●	
	SP8650B			●		600		●		45		●		●	
20	SP8657A	●				200	●			13	●		●		
	SP8657B			●		200	●			13	●		●		
	SP8658			●		200	●			30	●				●
32	SP8655A	●				200	●			13	●		●		
	SP8655B			●		200	●			13	●		●		
64	SP8755A	●				1200	●			75	●			●	
	SP8755B			●		1200	●			75	●			●	
100	SP8629			●		150	●	●		45	●				●

Ⓑ BINARY OUTPUTS

Variable-modulus prescalers

The two-modulus dividers will divide by either of two ratios according to the state of a control input compatible with ECL, TTL or CMOS as shown. Further division ratios can be obtained by means of extra prescalers. For example, by using the SP8790 (÷4) or SP8794 (÷8)— which are specially designed for extending the ratio of two-modulus dividers and have TTL compatible control inputs— it is possible to extend a ÷10/11 to 40/41 or 80/81 respectively.

Divide by	Type	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)			Max current (mA)	Control input		Output		Package		
		-55 +125	-40 +85	-30 +70	0 +70		5.0	5.2	6.8		TTL	ECL	TTL	ECL	Metal can	Ceramic	Plastic
3/4	SP8720A	●				300		●		65		●		●		●	
	SP8720B			●		300		●		65		●		●		●	
5/6	SP8740A	●				300		●		60		●		●		●	
	SP8740B			●		300		●		60		●		●		●	
6/7	SP8741A	●				300		●		60		●		●		●	
	SP8741B			●		300		●		60		●		●		●	
8/9	SP8691A	●				200	●	●		21		●	●	●		●	
	SP8691B			●		200	●	●		21		●	●	●		●	
	SP8743A	●				500		●		60		●		●		●	
	SP8743B			●		500		●		60		●		●		●	
10/11	SP8695A	●				200	●	●		21		●	●	●		●	
	SP8695B			●		200	●	●		21		●	●	●		●	
	SP8690A	●				200	●	●		21		●	●	●		●	
	SP8690B			●		200	●	●		21		●	●	●		●	
	SP8647A	●				250	●	●		65		●	●	●		●	
	SP8647B			●		250	●	●		65		●	●	●		●	
	SP8643A	●				350		●		65		●		●		●	
	SP8685A	●				500		●		65		●		●		●	
	SP8685B			●		500		●		65		●		●		●	
	SP8680A	●				550	●	●		111		●	●	●		●	
	SP8680B				●	575	●	●		111		●	●	●		●	

Variable-modulus prescalers (continued)

Divide by	Type	Temperature Range (°C)				Max frequency (MHz)	Supply voltage (V)			Max current (mA)	Control input		Output		Package		
		−55 +125	−40 +85	−30 +70	0 +70		5.0	5.2	6.8		TTL	ECL	TTL	ECL	Metal can	Ceramic	Plastic
20/22	SP8785A	●				1000		●		115		●		●		●	
	SP8785B			●		1000		●		115		●		●		●	
	SP8786A	●				1300		●		115		●		●		●	
	SP8786B			●		1300		●		115		●		●		●	
40/41	SP8793A	●				200		●		7	●		●			●	
	SP8793			●		225		●		7	●		●				●
	SP8716			●		520		●		11.2	●			*		●	
64/65	SP8718			●		520		●		11.2	●			*		●	
80/81	SP8792A	●				200		●		7	●		●			●	
	SP8792			●		225		●		7	●		●				●
	SP8719			●		520		●		11.2	●			*		●	
128/129	SP8703			●		1000	●			40	●			*		●	

*CMOS OUTPUT

Replacements

REPLACEMENTS FOR OBSOLETE AND NON-PREFERRED PRODUCTS IN THE SP8000 SERIES

OLD TYPE	NEW TYPE	NOTES	OLD TYPE	NEW TYPE	NOTES
SP8505	SP8630B		SP8647M	SP8647A	
SP8515	SP8630B		SP8650M	SP8650A	
SP8600M	SP8600A		SP8651A	SP8650A	
SP8601M	SP8601A		SP8651B	SP8650B	
SP8602M	SP8602A		SP8651M	SP8650A	
SP8603A	SP8602A		SP8652A	SP8650A	
SP8603B	SP8602B		SP8652B	SP8650B	
SP8603M	SP8602A		SP8652M	SP8650A	
SP8604M	SP8604A		SP8655M	SP8655A	
SP8605M	SP8605A		SP8657M	SP8657A	
SP8606M	SP8606A		SP8659M	SP8659A	
SP8607M	SP8607A		SP8660M	SP8660A	
SP8610M	SP8610A		SP8666B	SP8668B	
SP8613B...16B	(SP8610B)	1	SP8667B	SP8668B	
SP8613M...15M	(SP8610A)	1	SP8670M	SP8670A	
SP8617B	(SP8611B)	2	SP8671A	SP8670A	
SP8617M	(SP8611A)	2	SP8671B	SP8670B	
SP8619B	(SP8611B)	2	SP8671M	SP8670A	
SP8619M	(SP8611A)	2	SP8672A	SP8670A	
SP8620M	SP8620A		SP8672B	SP8670B	
SP8621A	SP8620A		SP8672M	SP8670A	
SP8621B	SP8620B		SP8675B	SP8678B	
SP8621M	SP8620A		SP8675M	SP8678M	
SP8622A	SP8620A		SP8676B	SP8678B	
SP8622B	SP8620B		SP8676M	SP8678M	
SP8622M	SP8620A		SP8677B	SP8678B	
SP8630M	SP8630A		SP8677M	SP8678M	
SP8631A	SP8630A		SP8685M	SP8685A	
SP8631B	SP8630B		SP8690M	SP8690A	
SP8631M	SP8630A		SP8695M	SP8695A	
SP8632A	SP8630A		SP8720M	SP8720A	
SP8632B	SP8630B		SP8736B	SP8735B	
SP8632M	SP8630A		SP8740M	SP8740A	
SP8636B	SP8635B		SP8741M	SP8741A	
SP8640A	SP8647A		SP8745	(SP8740)	3
SP8640B	SP8647B		SP8746	(SP8741)	3
SP8640M	SP8647A		SP8748	(SP8743)	3
SP8641A	SP8647A		SP8750B	(SP8755B)	4
SP8641B	SP8647B		SP8750M	(SP8755A)	4
SP8641M	SP8647A		SP8751B	(SP8755B)	4
SP8642A	SP8643A		SP8751M	(SP8755A)	4
SP8642B	SP8643A		SP8752B	(SP8755B)	4
SP8642M	SP8643A		SP8752M	(SP8755A)	4
SP8643B	SP8643A		SP8785M	SP8785A	
SP8643M	SP8643A		SP8786M	SP8786A	
SP8646A	SP8647A		SP8790M	SP8790A	
SP8646B	SP8647B		SP8794M	SP8794A	
SP8646M	SP8647A				

NOTES

1. New type operates from 5.2V power supply (instead of 7.4V).
2. New type operates from 5.2V power supply (instead of 6.8V).
3. New type is AC coupled and requires input capacitors.
4. New type operates from 5.0V instead of 6.8V and lacks VHF input.

The quality concept

In common with most semiconductor manufacturers, Plessey Semiconductors perform incoming piece parts check, in-line inspections and final electrical tests. However, quality cannot be inspected into a product; it is only by careful design and evaluation of materials, parts and processes - followed by strict control and ongoing assessment to ensure that design requirements are still being met - that quality products will be produced.

In line with this philosophy, all designs conform to standard layout rules (evolved with performance and reliability in mind), all processes are thoroughly evaluated before introduction and all new piece part designs and suppliers are investigated before authorisation for production use.

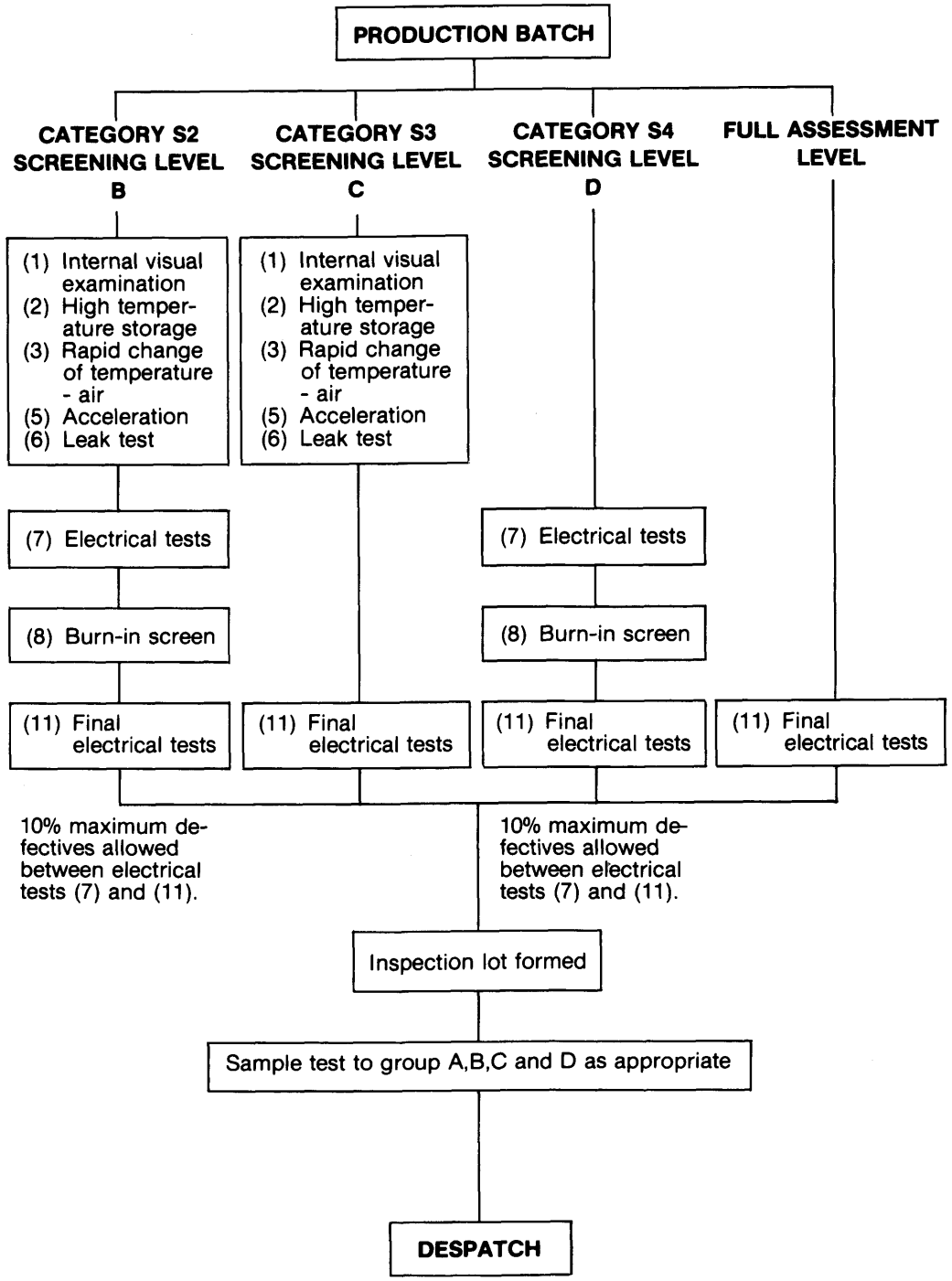
The same basic system of evaluation, appraisals and checks is used on all products up to and including device packing for shipment. It is only at this stage that extra operations are performed for certain customers in terms of lot qualification or release procedure.

By working to common procedures for materials and processes for all types of customers advantages accrue to all users - the high reliability user gains the advantage of scale hence improving the confidence factor in the quality achieved whilst the large scale user gains the benefits associated with basic high reliability design concepts.

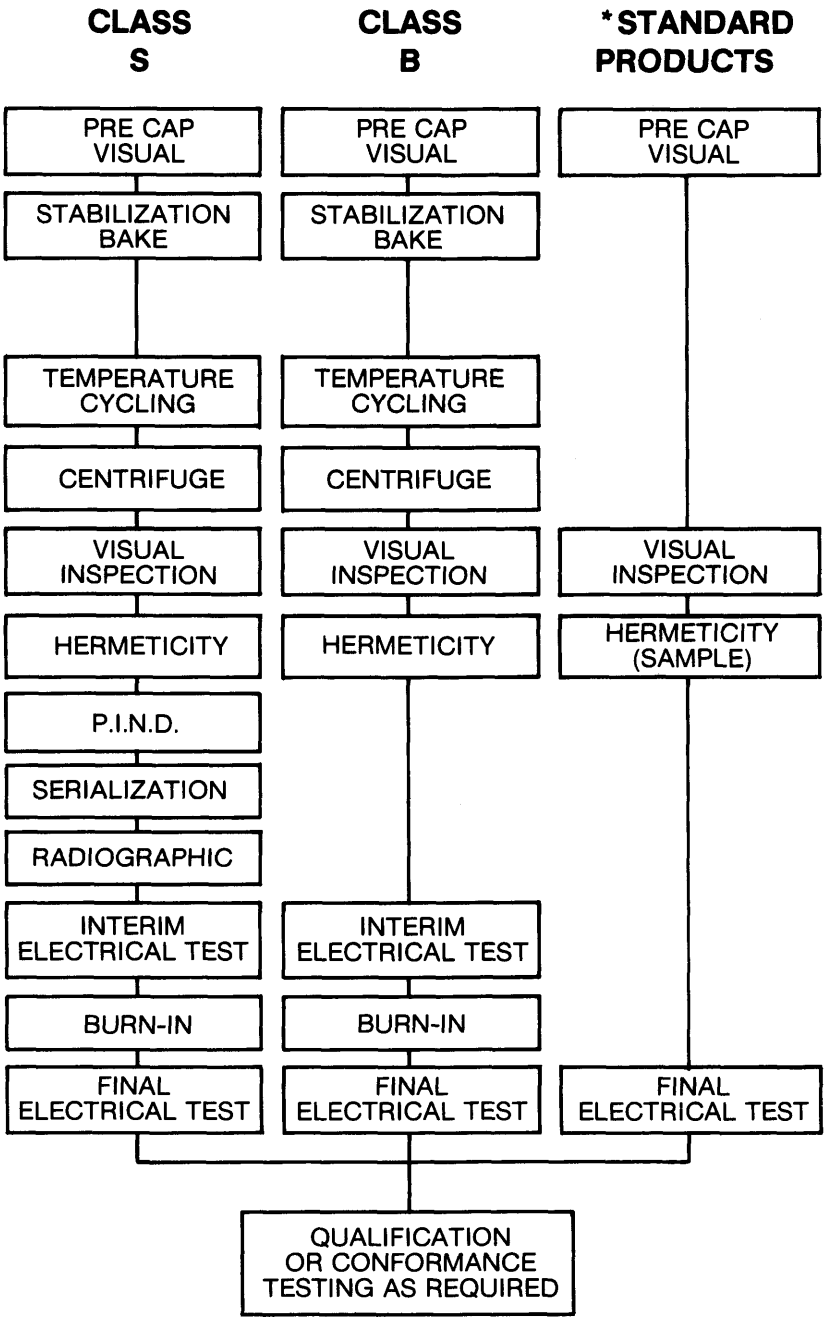
Plessey Semiconductors have the following factory approvals. **BS9300** and **BS9400** (BSI Approval No. 1053/M).
DEF-STAN 05-21 (Reg. No. 23HPOD).

In addition a number of U.S., European and British customers manufacturing electronics for space have approved our facilities.

Screening to BS9400



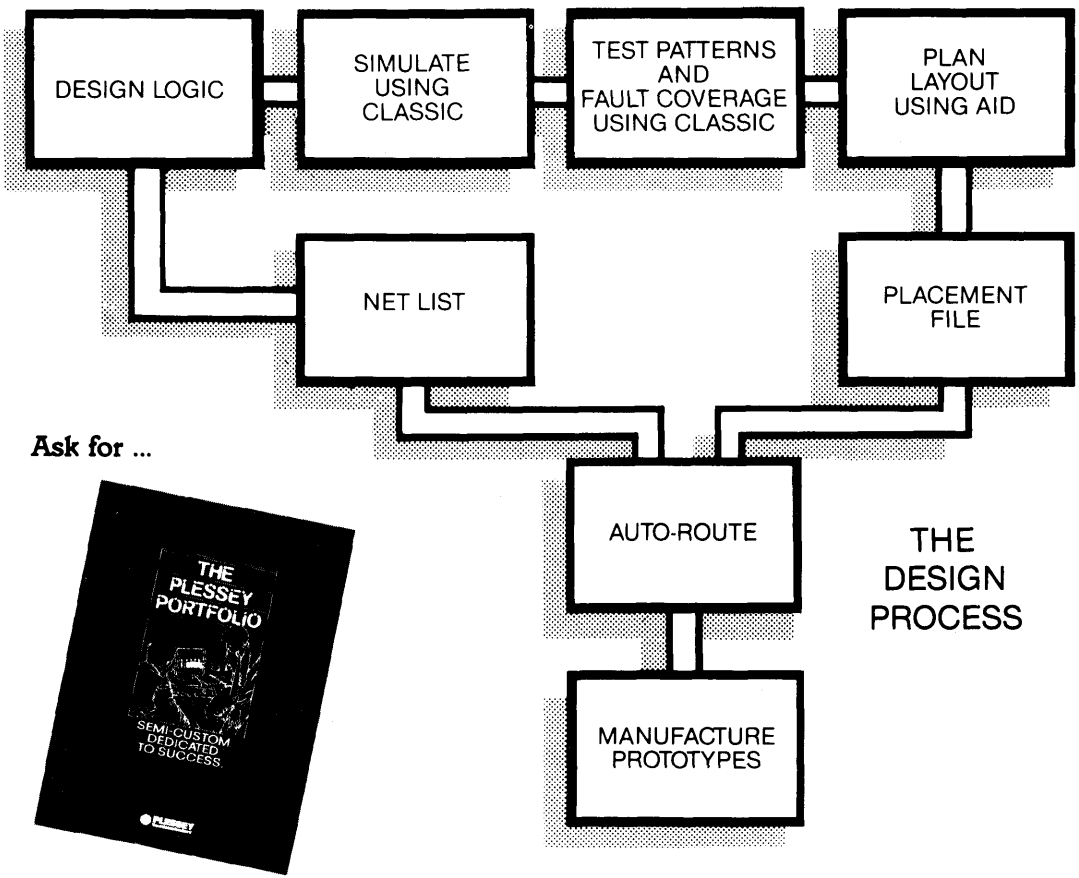
Plessey Hi-Rel screening



*Plessey Semiconductors reserve the right to change the Screening Procedure for Standard Products.

Semi-custom

Plessey Semiconductors' advanced work in the Semi-Custom field enables us to offer our customers the opportunity to develop their own high performance circuits using our CLASSIC software. Among the many advantages are:
• CLASSIC is cost effective and user friendly • Prototypes in as little as 3 weeks • Close coordination with customer throughout design and production process • State-of-the-art high performance produces • Up to 10044 gates available



Ask for ...

Microgate-C (Si-Gate CMOS)

CLA 2000 SERIES

- Double layer metallisation
- 5 micron channel length
- Product family:
  CLA 21XX 840 Gates
  CLA 23XX 1400 Gates
  CLA 25XX 2400 Gates
- 7ns max. prop delay (2 input NAND fanout of 2 with 2mm track 0-70° C 4.5-5.5V)
- 14MHz system clock rate
- 30MHz toggle rate
- Fully auto-routed

CLA 3000 SERIES

- Double layer metallisation
- 4 micron channel length
- Product family:
  CLA 31XX 840 Gates
  CLA 33XX 1440 Gates
  CLA35XX 2400 Gates
  CLA 37XX 4200 Gates
  CLA 39XX 6000 Gates
- 5ns max. prop delay
- 20MHz system clock rate
- 50MHz toggle rate
- Fully auto-routed

CLA 5000 SERIES

- Double layer metallisation
- 2 micron channel length
- Product family:
  CLA 51XX 640 Gates
  CLA 52XX 1232 Gates
  CLA 53XX 2016 Gates
  CLA 54XX 3060 Gates
  CLA 55XX 4408 Gates
  CLA 56XX 5984 Gates
  CLA 58XX 8856 Gates
  CLA 59XX 10044 Gates
- 2.5ns max. prop delay
- 40MHz system clock rate
- 100MHz toggle rate
- Fully auto-routed

Microcell

MJ1000 5 micron NMOS Up to 3000 equivalent gates

The care and feeding of High Speed Dividers

High Speed Divider Integrated Circuits are seeing increasing areas of application. Limited at one time to high cost military applications, low cost devices operating up to 2GHz are now available. At these frequencies circuit design and layout owe much more to analogue RF design techniques than normal digital ones and the limitations on flexibility and component choice inherent in UHF RF design are of paramount importance in successful designs.

PRACTICAL DESIGN CONSIDERATIONS

High speed divider applications require the printed circuit boards to be mechanically designed with two considerations in mind:

(1) Electrical performance
(2) Mechanical and thermal performance.

These two considerations are inter-related; for example, the use of 1/16 inch thick fibreglass PC board may be desirable mechanically, but a 50Ω stripline on this thickness of board is about 5/32 inch wide, and is thus too wide to pass between the pins of an IC.

Most of the heat conducted from a dual-in-line IC package is removed from the bottom of the package. Less than 10 % is conducted out by the leads, and because of the cavity between the chip and lid, relatively little through the top of the package.

For this reason, the use of a double-layer PC board layout is recommended, with a ground plane top surface. Where 1/32 inch thick material is used, a top surface ground plane will add substantially to the heat dissipation capabilities of the board.

For use at very high frequencies, consideration must be given to the type of component used. Carbon composition resistors are more nearly resistive at high frequencies than either carbon or metal film types, and are available in very small sizes. Bypass capacitors need to be chosen carefully if they are to act as low impedances, as series inductance leads to an increasing impedance with frequency above the series resonant frequency of the device. As a guide, a 1000pF disc ceramic capacitor with 1/4 inch leads will be self resonant at about 75MHz, and will appear as an inductive impedance of about 22Ω at 800MHz. The use of chip capacitors is recommended above 500MHz, although leaded monolithic ceramic capacitors with suitably short leads are often acceptable.

The use of a ground plane for RF decoupling purposes is often recommended, and can be helpful. However, the danger is that the ground current paths in the plane are not defined very well, and because of this lack of definition, the ground plane can cause unsatisfactory operation. Probably the best method is to return all the bypass capacitors to a single point (as in Fig.1) and return this point to the ground plane.

Also note that in Fig.1 the output load resistors have their grounded ends connected together and a common return used. Because the currents in the resistors are in antiphase, cancellation of the inductive effects taken place, and the path followed by the relatively large output currents is controlled. Defining the ground current path is more important in applications like frequency synthesis, where a relatively large part of the system may be on one PCB.

It is well known that the effect of mismatching a transmission line is to cause variations in the voltage along the line. Standard practice at Plessey Semiconductors has been to use a 5:1 attenuator manufactured from 'microdot' resistors as an attenuator feeding a 50Ω sampling oscilloscope or a power meter. Although a high VSWR will exist on the line from the generator to the test fixture, the theory is that the line from the power meter to the attenuator will be a matched line, and so the power measured is 14dB lower than the power at the device input pin.

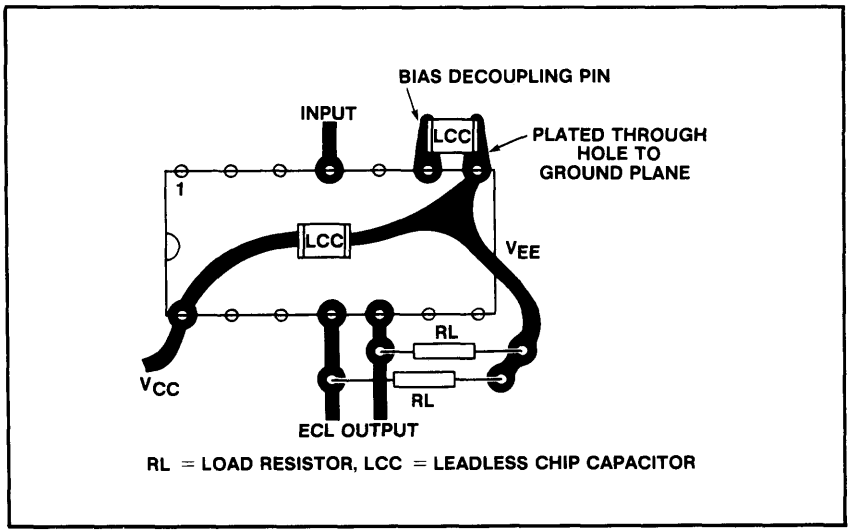


Fig.1 Single point grounding

This method has been proved very successful, even if simple, and offers some advantages over the use of hybrids or directional couplers.

The use of a matched 50Ω system can help, and using microstrip techniques, a track with a defined impedance is reasonably practical. The impedance of a microstrip line is given by:

$$Zo = 377\ (L/w)\ (1/\varepsilon_r)$$

Where L = dielectric thickness, w = width of track and ε_r is the relative permeability of the board material.

Some correction factors have to be applied, and typically, on 1/16 inch glass fibre epoxy board, the following sizes provide a guide to track width

100Ω - 1mm
75Ω - 2mm
50Ω - 4mm

These impedances rely on the ground plane on the obverse of the board being complete, and where boards are wave soldered, it may be necessary to make arrangements to prevent blistering.

The input level of a divider should be maintained within the guaranteed operating window shown on its data sheet (Fig.2). Excessive input can vary in its effects, from causing permanent damage to miscounting, especially when cold. Running the device at too low a level can cause problems, even though the level is within the 'typical' performance line of the device. An ECL output signal on pin 6 of the device in Fig.3 can couple 60mV of signal to the input shown on Fig.2 at 500MHz. Such a level of coupling can lead to divider jitter if the input signal is low, and it becomes very necessary to keep the inputs and outputs well separated at the higher frequencies. This includes ECL lines to modulus control pins on two modulus dividers.

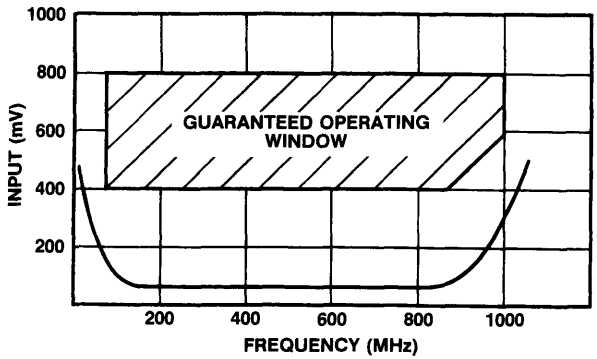


Fig.2 Example of input sensitivity curves

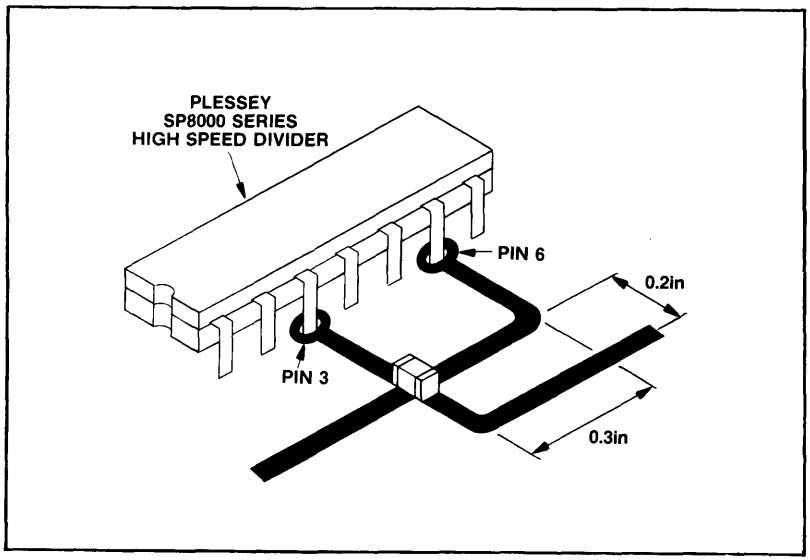


Fig.3 Coupling between parallel traces

Most dividers are edge triggered, and although they are specified over a frequency range with sine wave input, they will operate to lower frequencies provided a suitably high slew rate is provided on the input signal. This is generally of the order of 100 to 200 volts/microsecond. This should be achieved by shaping of the input signal, for example by limiting, rather than by overdriving the device.

The outputs of devices may be of the following forms:

(1) ECL
(2) Open collector TTL
(3) TTL
(4) CMOS

Of these, the ECL output is well defined; some devices require external load resistors and the data sheet should be consulted. Where these external resistors are required, suitable interconnection techniques should be used between them and the device; the resistors should be carefully chosen for their non-inductive properties when output frequencies are very high. Where an ECL output divider drives another divider it is best to AC couple, since few dividers are strictly ECL-compatible on their inputs.

Open collector TTL outputs are relatively slow. Although the negative edge is limited in speed by the turn-on time of the output transistor, the rising edge is limited by the external load resistor and capacitance to ground. In practice this means that short narrow tracks are required to the following device, and a minimum 'fan-in' load provided. In addition, open collector TTL should not be used above about 10MHz output frequency.

True TTL outputs are not so limited, because of the active pull-up. Nevertheless, the use of such outputs at frequencies above about 25-30MHz is not recommended, especially into capactive loads. Loads of more than 30pF should not be driven faster than about 15MHz. Note that the current drawn by true TTL outputs increases with increasing load capacitance.

CMOS outputs are, on the face of it, TTL-compatible. However, investigation will show that the outputs are not guaranteed to meet TTL levels at TTL currents and it is not recommended that CMOS output devices be used to directly drive TTL. Where an interface of this sort is required, an active transistor interface should be used.

Fig.4 shows a circuit for an ECL-TTL interface, using a line receiver. Simple circuits using one or two transistors cannot be guaranteed to work over all the tolerances of ECL output voltages and temperature ranges.

Interfacing to dividers is not difficult if a few simple rules are obeyed. These are:

(1) Observe the input requirements - guaranteed input operating area, and slew rate.
(2) Do not use open collector outputs above 10MHz.
(3) Do not use CMOS outputs to drive TTL.
(4) Use a sensible layout with good components, and sensible values - 0.1 microfarad ceramic capacitors are NOT bypasses at 1.5GHz.

Treating dividers as RF linear devices is probably the best way to ensure successful applications at high frequencies. There is no magic in HF design, only intelligent layout and sensible component choice.

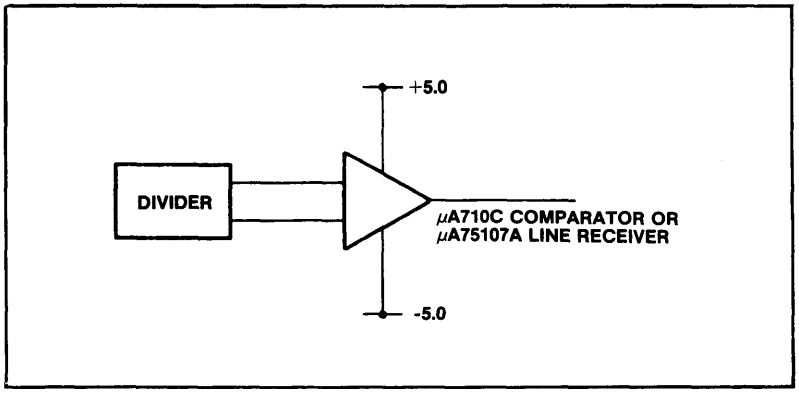


Fig.4 ECL/TTL interface

Impedance Matching

The use of microstrip techniques has been mentioned already. However, in itself this will not produce a matched network and various possibilities exist to improve the matching at the input of a device. These include Tchebycheff impedance transforming networks, narrow band 'L' matching networks, and at high enough frequencies, the use of transmission lines. Wideband matching is often difficult, and attempts should be made to use networks that have the lowest possible working Q. This is for two reasons: firstly a high Q network will not only be narrow band, but will have the capability of increasing the losses, and secondly, a low Q network is generally more tolerant of component variations.

The greater losses in high Q circuits occur because of the greater circulating current: the loss power is I^2R, so that if the Q is doubled with all else constant, the power loss is increased by 4 times.

The easiest method of determining matching components is by means of the Smith Chart.

THE SMITH CHART

The input impedance of SP8000-series high speed dividers varies as a function of frequency and is therefore specified on the datasheets by means of Smith Charts. The following information is included in this handbook as a guide to their interpretation and use.

Construction of the chart

The chart is constructed with two sets of circles, one set comprising circles of CONSTANT RESISTANCE (Fig. 5) and the other circles of CONSTANT REACTANCE (Fig. 6). The values on these circles are normalised to the characteristic impedances of the system by dividing the actual value of resistance or reactance by the characteristic impedance e.g. in a 50Ω system, a resistance of 100Ω is normalised to a value of 2.0.

By combining Figs. 5 and 6 to form Fig. 7, a chart is produced in which any normalised impedance has a unique position on the chart, and the variation of this impedance with frequency or other parameters may be plotted.

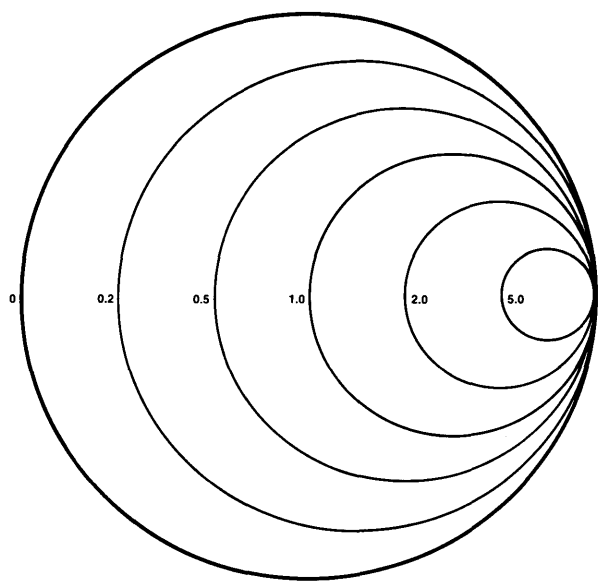


Fig.5 Constant resistance circles

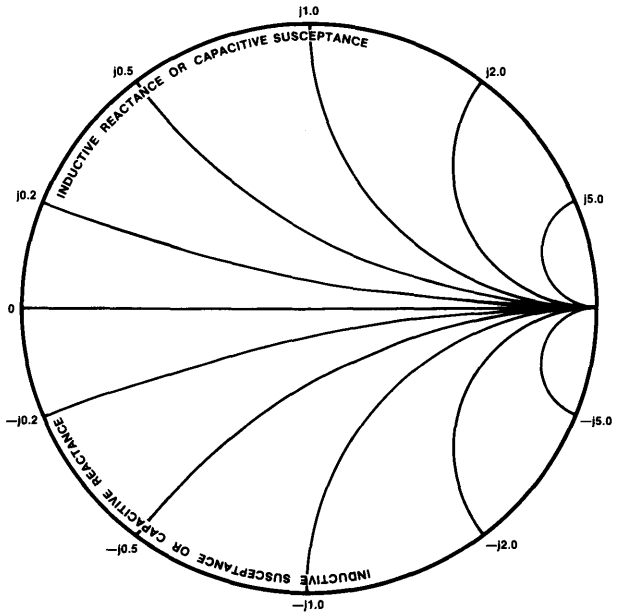


Fig.6 Constant reactance circles

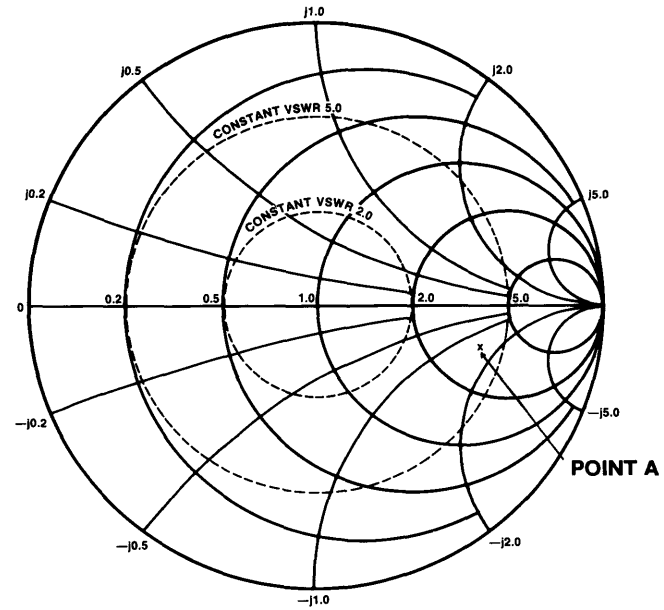


Fig.7 The complete chart

A further series of circles may be plotted on the chart: these are circles of constant VSWR, and represent the degree of mismatch in a system. The VSWR is the ratio of the device impedance to the characteristic impedance, and is always expressed as a ratio greater than 1: thus a 25Ω device in a 50Ω system gives rise to a 2:1 VSWR. These circles of constant VSWR have been added in Fig. 7.

Any point can be represented on the Smith Chart: for example an impedance of 150-*j*75Ω can be represented by a normalised impedance (in a 50 Ω system) of 3-*j*1.5 and this point is plotted in Fig.7 as point A.

Network calculations

The main application for Smith Charts with integrated circuits is in the design of matching networks. Although these can be calculated by use of the series to parallel (and vice-versa) transforms, followed by the application of Kirchoff's Laws, the method can be laborious. Although the Smith Chart as a graphical method cannot necessarily compete in terms of overall accuracy, it is nevertheless more than adequate for the majority of problems, especially when the errors inherent in practical components are taken into account.

Any impedance can be represented at a fixed frequency by a shunt conductance and susceptance (impedances as series reactance and resistance in this context). By transferring a point on the Smith Chart to a point at the same diameter but 180° away, this transformation is automatically made (see Fig. 8) where A and B are the series and parallel equivalents.

It is often easier to change a series RC network to its equivalent parallel network for calculation purposes. This is because as a parallel network of admittances, a shunt admittance can be directly added, rather than the tortuous calculations necessary if the series form is used. Similar arguments apply to parallel networks, so in general it is best to deal with admittances for shunt components and reactances for series components.

Admittances and impedances can be easily added on the Smith Chart (see Fig. 9). Where a series inductance is to be added to an admittance (i.e. parallel R and C), the admittance should be turned into a series impedance by the method outlined above and in Fig. 8. The series inductance can then be added as in Fig. 9 (see also Fig. 10).

Point A is the starting admittance consisting of a shunt capacitance and resistance. The equivalent capacitive impedance is shown at point B. The addition of a series inductor moves the impedance to point C. The value of this inductor is defined by the length of the arc BC, and in Fig. 10 is -*j*0.5 to *j*0.43 i.e. a total of *j*0.93. This reactance must of course be denormalised before evaluation. Point C represents an inductive impedance which is equivalent to the admittance shown at Point D. The addition of shunt reactance moves the input admittance to the centre of the chart, and has a value of -*j*2.0. Point D should be chosen such that it lies on unity impedance/conductance circle: thus a locus of points for point C exists.

This procedure allows for design of the matching at any one frequency. Wide band matching is more difficult and other techniques are needed. Of these, one of the most powerful is to absorb the reactance into a low pass filter form of ladder network: if the values are suitably chosen, the resulting input impedance is dependent upon the reflection coefficient of the filter.

At frequencies above about 400MHz, it becomes practical to use sections of transmission line to provide the necessary reactances, and reference to one of the standard works on the subject is recommended.

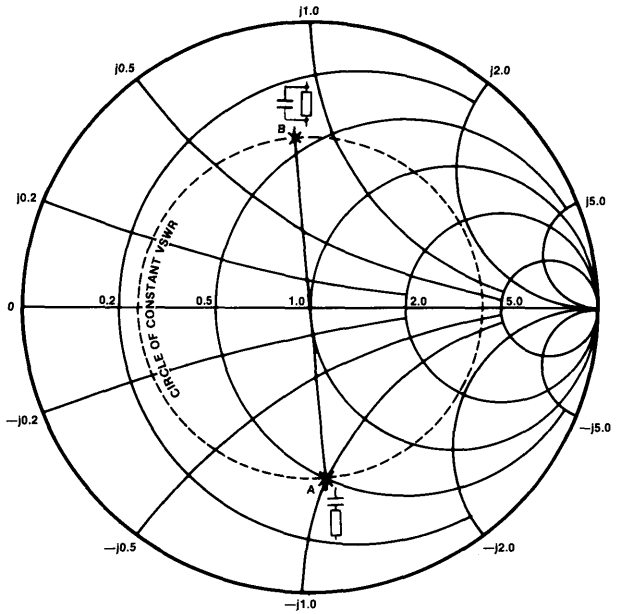


Fig.8 Series reactance to parallel admittance conversion

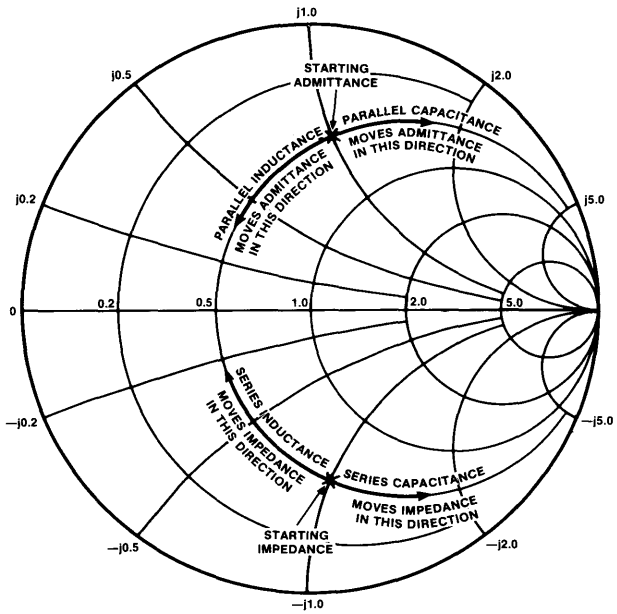


Fig.9 Effects of series and shunt reactance

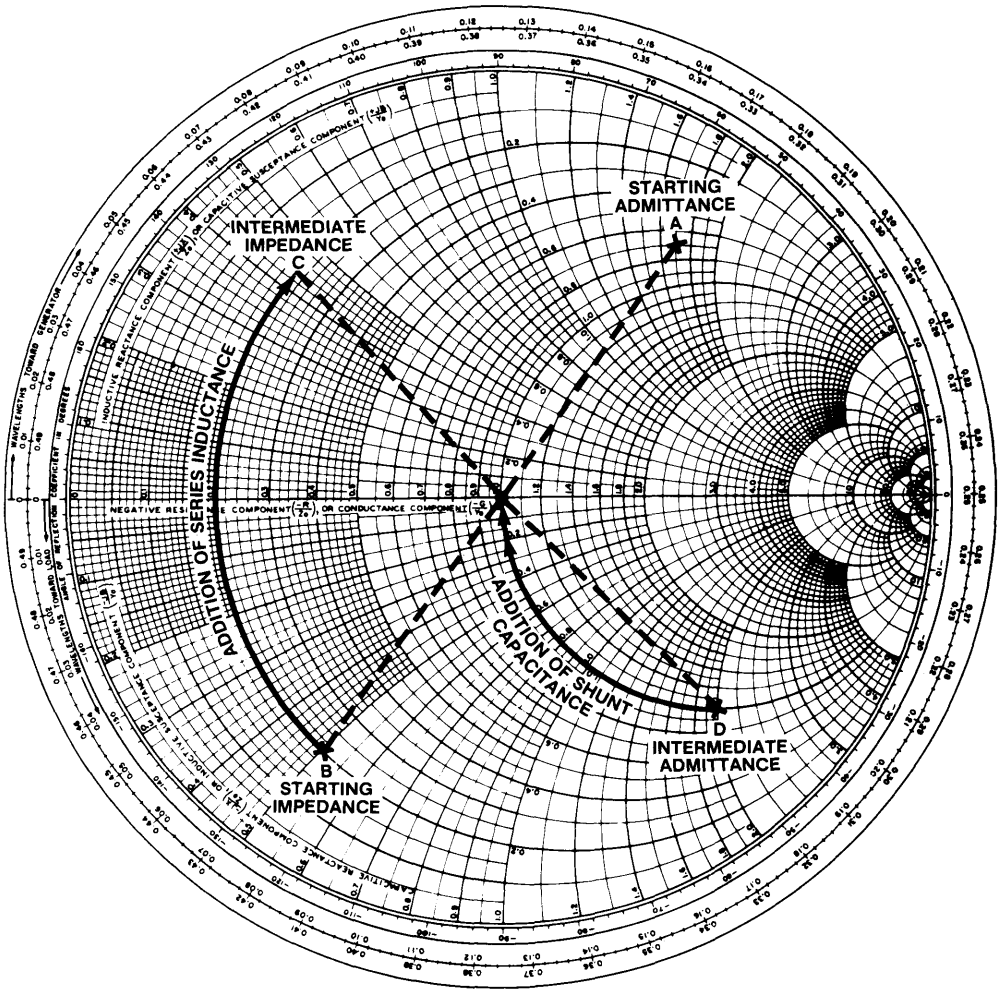


Fig.10 Matching design using the Smith Chart

PHASE NOISE AND DIVIDERS

Phase noise is becoming increasingly important in systems and it is necessary to minimise its effects. First, however, phase noise must be defined.

A spectrally pure signal of a given frequency would appear on a perfect spectrum analyser display as a single straight line as in Fig.11. If the signal is frequency modulated with a discrete modulation frequency, the result will be a comb of frequencies as in Fig.12, while modulation with noise will produce an output spectrum as in Fig.13. Note that the noise density decreases as the offset from the carrier increases. This effect is the result of the effectively lower modulation index m. In the case of a Voltage Controlled Oscillator modulated by white noise, a similar effect will be seen, because for a given deviation f, the modulation index m, ($= 1/fmod$) is greater for lower frequencies than for higher frequencies. Thus the number of sidebands is greater for lower frequencies, and the noise spectral density increases as the carrier is approached.

The causes of phase noise in dividers are not well understood, but the effects of internal noise on the switching point of the various flip-flops cannot be ignored. The $1/f$ noise will obviously inter-relate to the phase noise if this is so, and it is interesting to note that various measurements of Gallium Arsenide dividers suggest performances 20 to 30dB worse than for

ECL dividers. Rohde (ref. 4) suggests that TTL and CMOS are much better than ECL, although little work has been published in this field, possibly because of the measurement difficulties.

The non-saturating nature of ECL, the fact that the transistors are designed and processed for high speed rather than low noise, and the smaller signal swings than TTL or CMOS, lead intuitively to the conclusion that ECL should be worse than either of these other two logic families. This appears to be the case, while the high 1/*f* noise knee of Gallium Arsenide devices leads to the high relatively close in phase noise.

Devices with slow output edges, such as open collector TTL output stages may also be expected to be worse, which is again born out in practice.

Minimisation of phase noise requires the use of well-filtered supplies, correct input levels and minimisation of noise in level changing circuitry.

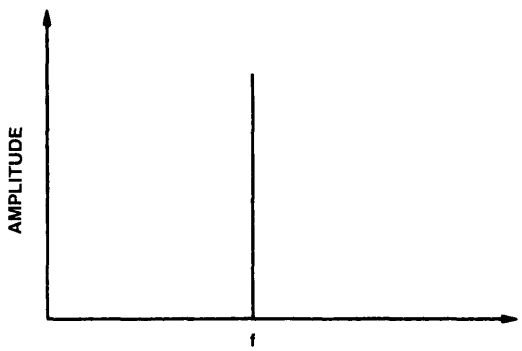


Fig.11 Spectrally pure signal

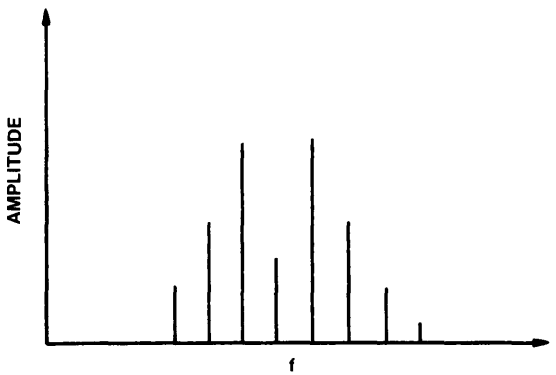


Fig.12 Spectrally pure signal, frequency modulated with single tone

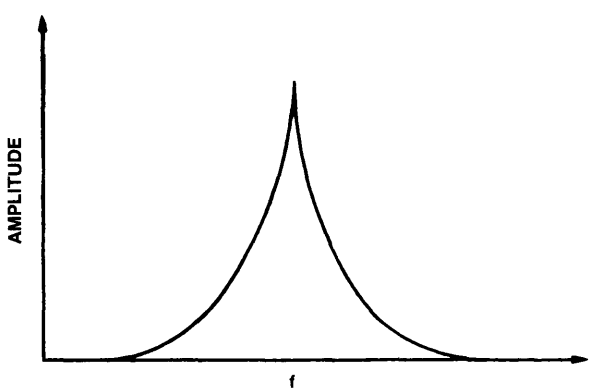


Fig.13 Spectrally pure signal, frequency modulated by noise

THERMAL DESIGN

The temperature of any semiconductor device has an important effect upon its long term reliability. For this reason, it is important to minimise the chip temperature; and in any case, the maximum junction temperature should not be exceeded.

Electrical power dissipated in any device is a source of heat. How quickly this heat can be dissipated is directly related to the rise in chip temperature: if the heat can only escape slowly, then the chip temperature will rise further than if the heat can escape quickly. To use an electrical analogy: energy from a constant voltage source can be drawn much faster by using a low resistance load than by using a high resistance load.

The thermal resistance to the flow of heat from the semiconductor junction to the ambient temperature air surrounding the package is made up of several elements. These are the thermal resistance of the junction-to-case, case-to-heatsink and heatsink-to-ambient interfaces. Of course, where no heatsink is used, the case-to-ambient thermal resistance is used.

These thermal resistances may be represented as

$\theta_{ja} = \theta_{jc} + \theta_{ch} + \theta_{ha}$

where θ_{ja} is thermal resistance junction to ambient °C/W
θ_{jc} is thermal resistance junction-to-case °C/W
θ_{ch} is thermal resistance case-to-heatsink °C/W
θ_{ha} is thermal resistance heatsink-to-ambient °C/W

The temperature of the junction is also dependent upon the amount of power dissipated in the device — so the greater the power, the greater the temperature.

Just as Ohm's Law is applied in an electrical circuit, a similar relationship is applicable to heatsinks.

$T_j = T_{amb} + P_D (\theta_{ja})$
T_j = junction temperature
T_{amb} = ambient temperature
P_D = dissipated power

From this equation, junction temperature may be calculated, as in the following examples.

Example 1

An SP8785B is to be used at an ambient temperature of +50° C. From Table I, θ_{ja} for the DG14 package is 110° C/W; from the datasheet, P_D = 598mW and T_j max = 175° C.

$T_j = T_{amb} + P_D \theta_{ja}$
$= 50 + (0.598 \times 110)$
$= 115.8°$ C (typ.)

Where operation in a higher ambient temperature is necessary, the maximum junction temperature can easily be exceeded unless suitable measures are taken:

Example 2

An SP8785A (T_j max. = +175° C) is to be used at an ambient temperature of +120° C. Again, θ_{ja} = 110° C/W, P_D = 598mW.

$T_j = 120 + (0.598 \times 110)$
$= +185.8°$ C (typ.)

This clearly exceeds the maximum permissible junction temperature and therefore some means of decreasing the junction-to-ambient thermal resistance is required.

As stated earlier, θ_{ja} is the sum of the individual thermal resistances; of these, θ_{jc} is fixed by the design of device and package and so only the case-to-ambient thermal resistance, θ_{ca}, can be reduced.

If θ_{ca}, and therefore θ_{ja}, is reduced by the use of a suitable heatsink, then the maximum T_{amb} can be increased:

Example 3

Assume that an IERC LIC14A2U dissipator and DC000080B retainer are used. This device is rated as providing a θ_{ja} of 55° C/W for the DG14 package. Using this heatsink with the SP8785A operated as in Example 2 would result in a junction temperature given by:

$$T_j = 120 + (0.598 \times 55)$$
$$= 152.9° C$$

Nevertheless, it should be noted that these calculations are not necessarily exact. This is because factors such as θ_{jc} may vary from device type to device type, and the efficacy of the heatsink may vary according to the air movement in the equipment.

In addition, the assumption has been made that chip temperature and junction temperature are the same thing. This is not strictly so, as not only can hot spots occur on the chip, but the thermal conductivity of silicon is a variable with temperature, and thus the θ_{jc} is in fact a function of chip temperature. Nevertheless, the method outlined above is a practical method which will give adequate answers for the design of equipment.

It is possible to improve the dissipating capability of the package by the use of heat dissipating bars under the package, and various proprietary items exist for this purpose.

Under certain circumstances, forced air cooling can become necessary, and although the simple approach outlined above is useful, more factors must be taken into account.

Thermal resistance in still air (° C/W) (Note 1)		
Package type	θ_{ja}	θ_{jc}
14-lead ceramic DIL, metal lid (DC14)	100	25
8-lead ceramic DIL (DG8)	150	40
14-lead ceramic DIL (DG14)	110	30
16-lead ceramic DIL (DG16)	110	30
8-lead plastic DIL (DP) (Note 2)	200	-
14-lead plastic DIL (DP14) (Note 2)	160	-
16-lead plastic DIL (DP16) (Note 2)	165	-
8-lead TO-5 (CM8)	210	60

NOTES

1. Measurements were made on a printed circuit board with no contact between the bottom of the package and the board.
2. Measurements for plastic DIL packages were made using packages with Kovar lead frames and eutectic die bonds.

Table 1 Thermal resistance values for different packages

REFERENCES

1. Electronic Applications of the Smith Chart, Philip H. Smith, McGraw Hill, 1969.
2. Microwave Filters, Impedance - Matching Networks and Coupling Structures, Matthei, Young, Jones, Artech House 1980. SBN 0890060991.
3. Tables of Chebyshev Impedance Transforming Networks of Low Pass Filter Form, Matthei G.L., Proc IEEE August 1964 pp 939 - 963.
4. Digital PLL Frequency Synthesis Theory and Design V.L. Rohde, Prentice Hall 1983 ISBN 0-13-214239-2.

Technical Data

PLESSEY
Semiconductors

SP8600A & B

250MHz ÷ 4

The SP8600 is an asynchronous ECL counter with open collector outputs. It requires external input bias and an AC coupled input signal of 600mV p-p.

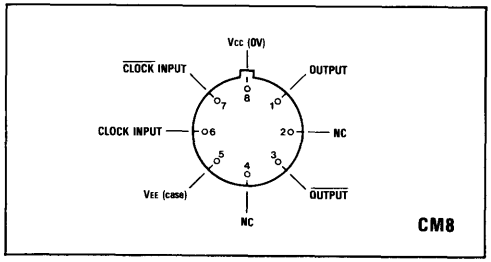


Fig.1 Pin connections - bottom view

FEATURES

- Open Collector Output
- AC Coupled Input

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 85mW
- Max. Input Frequency: 250MHz
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -10V
- Output Voltage (Pins 1 and 3): V_{EE} +14V
- Storage Temperature Range: -55°C to +175°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

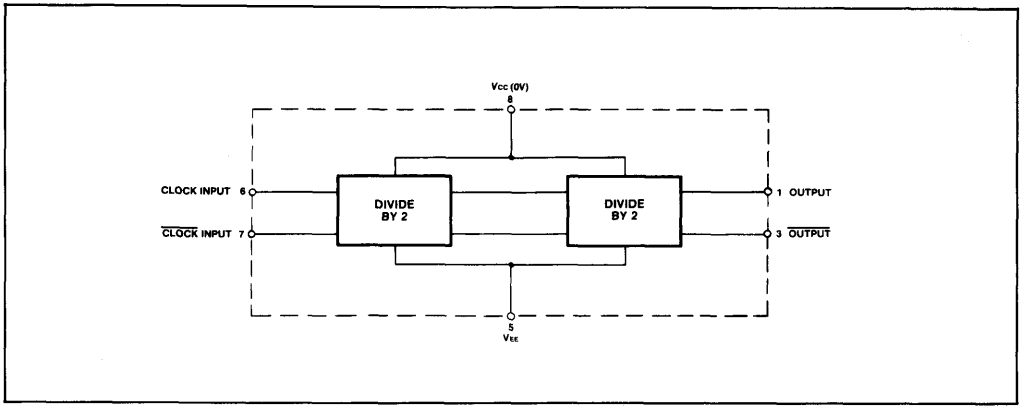


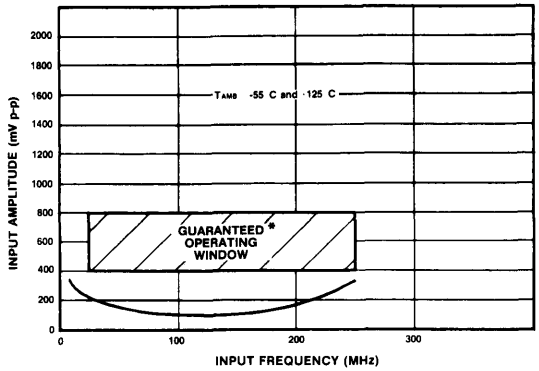
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{EE} = -5.2V ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV
Minimum frequency (sinewave input)	f_{min}		25	MHz	Input = 400-800mV
Power supply current	I_{EE}		25	mA	V_{EE} = -5.2V
Output current	I_{OUT}	1.65		mA	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig. 5.



*Tested as specified above.

Fig.3 Typical input characteristics of SP8600A

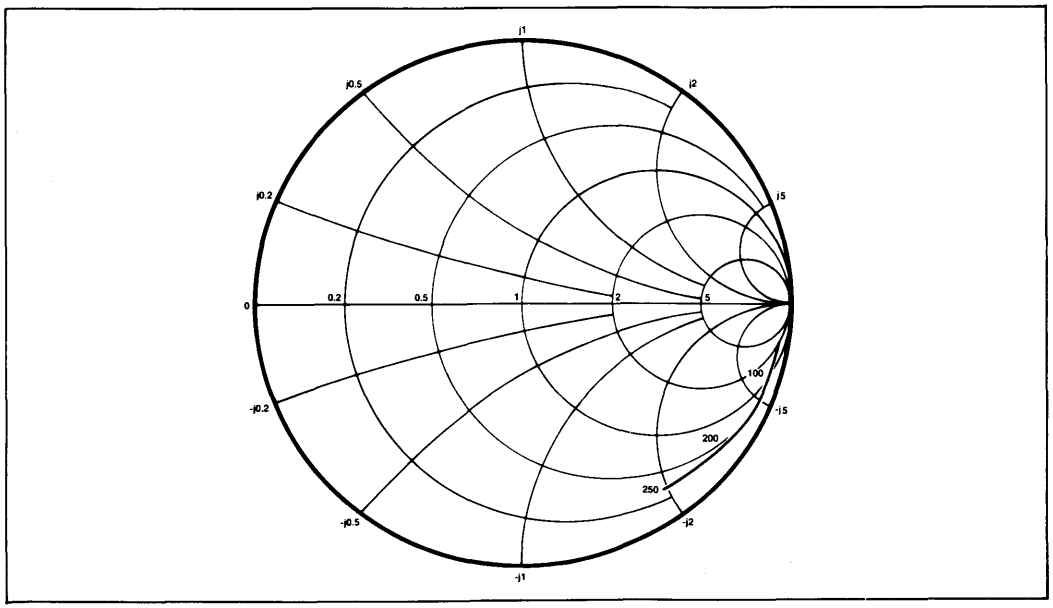


Fig.4 Typical input impedance: supply voltage -5.2V, temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The input is normally AC coupled to one of the inputs or, if complementary signals are available, to both inputs. The inputs require an external bias as shown in Fig.5.
2. If no signal is present the device will self-oscillate. If this is undesirable this can be prevented by offsetting the two inputs by approximately 40mV as shown in Fig. 6.
3. The outputs are in the form of complementary free collectors with about 2mA available from them over full temperature range. The outputs can be interfaced to ECL or Schottky TTL as shown in Fig. 7.
4. For maximum frequency operation the output load resistor values must be such that the output transistors will not saturate. If the output load resistors are connected to 0V then saturation occurs with resistor values greater than 600 ohms. If only one output is used the other output can be connected to 0V.
5. The input can be operated down to DC but input slew rate must be better than 20V/µs.
6. The input impedance varies as a function of frequency. See Fig. 4.

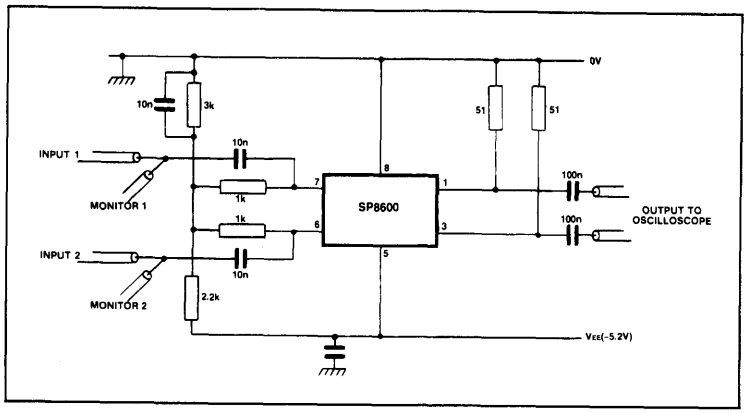


Fig.5 Test circuit

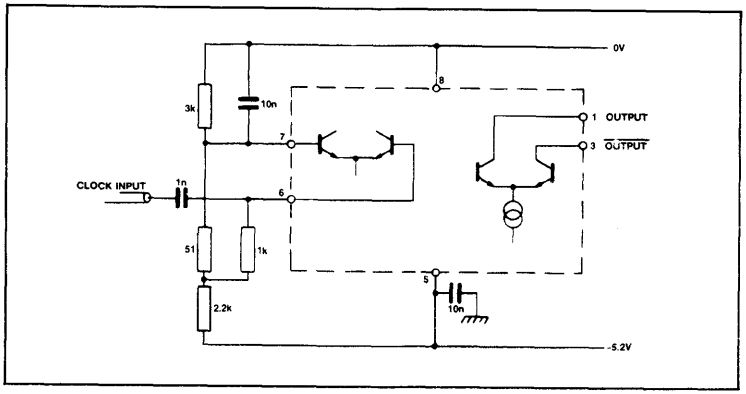


Fig.6 Biasing to prevent oscillation under no signal conditions

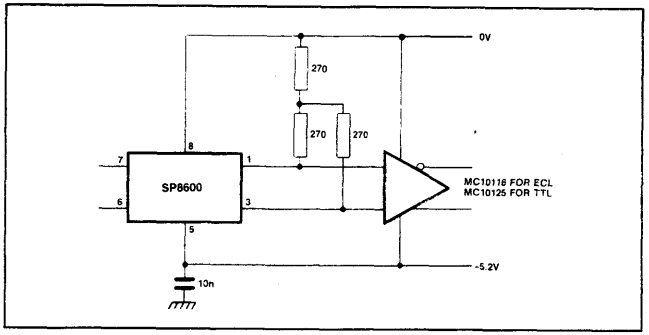


Fig.7 Interfacing to ECL and Schottky TTL

PLESSEY
Semiconductors

SP8601A & B

150MHz ÷ 4

The SP8601 is an asynchronous ECL counter with a current steered output which can be used to drive TTL or CMOS. Biased externally, it may be directly driven from an ECL II source.

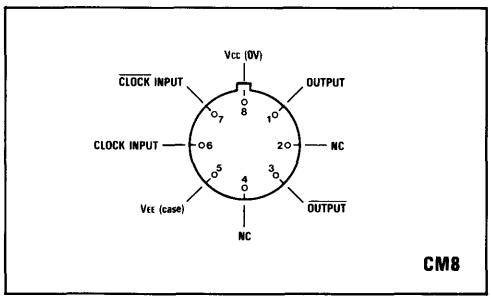


Fig.1 Pin connections - bottom view

FEATURES

- Current steered output can drive TTL or CMOS
- AC or DC Coupled Input
- Inputs ECL II Compatible

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 85mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -10V
- Output Voltage (Pins 1,3): V_{EE} +14V
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

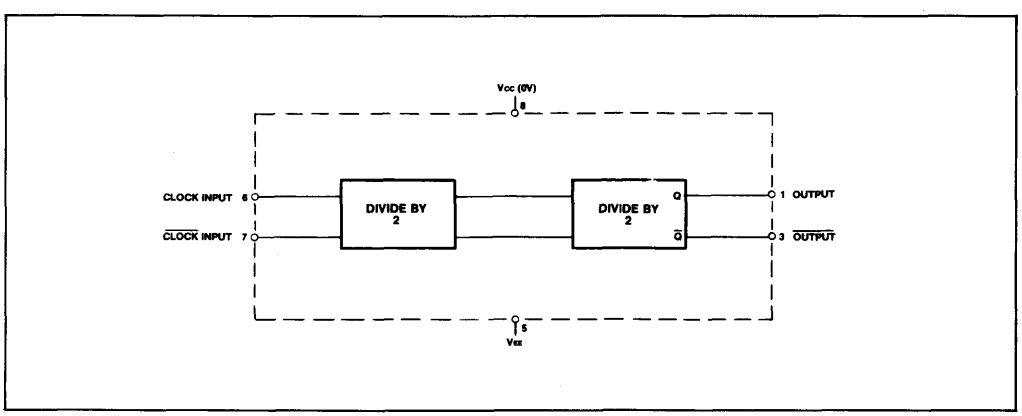


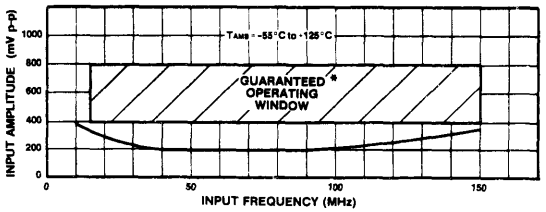
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{max}	150		MHz	Input = 400-800mV p-p
Minimum frequency (sinewave input)	f_{min}		15	MHz	Input = 400-800mV p-p
Power supply current	I_{EE}		25	mA	V_{EE} = -5.2V
Output current	I_{OUT}	1.6		mA	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig. 5.



*Tested as specified above.

Fig.3 Typical characteristic of SP8601A

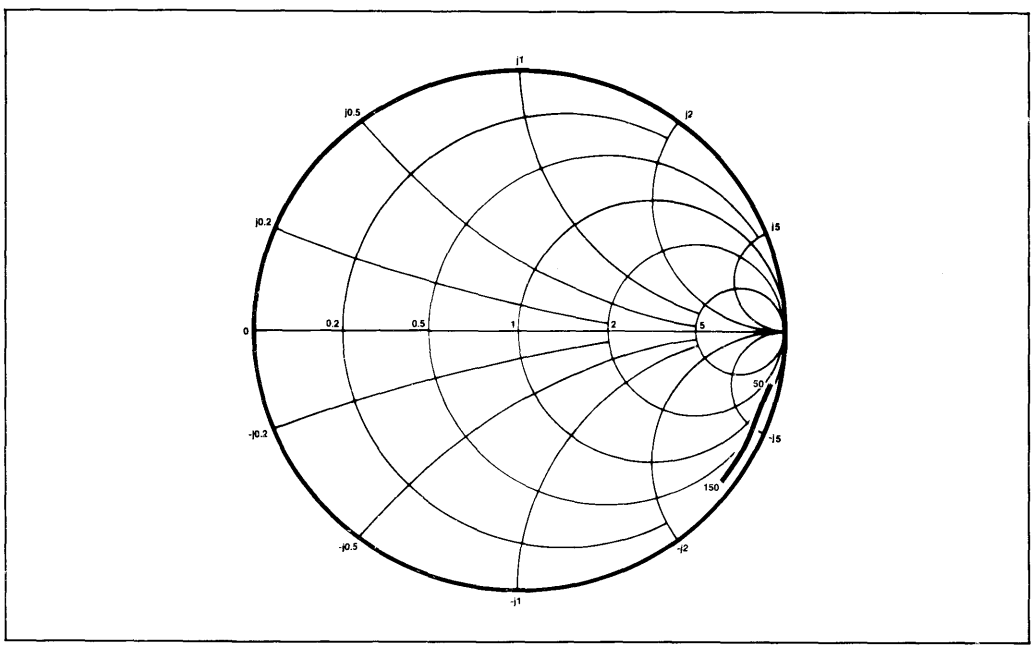


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The signal source can be capacitively coupled to the clock input if input bias is provided (See Fig. 6) but is normally directly coupled with ECL II levels. The inputs can be operated either singly or with double complementary input drive.
2. The outputs are in the form of complementary free collectors with 1.6mA available from them over full military temperature range (A grade). The outputs can be interfaced to ECL or Schottky TTL as shown in Fig. 5. Interfacing to TTL at frequencies above 20MHz requires low capacitance interconnections and the use of Schottky TTL.
3. For maximum frequency operation the output load resistor values must be such that the output transistors will not saturate. If the output load resistors are connected to 0V then saturation will occur with resistor values greater than 600 ohms. If only one output is used the other output can be connected to 0V. See Table 1 for typical variation of maximum input frequency with output load resistor.

Minimum Output Voltage (mV)	Load Resistor (ohms)	Input Frequency (MHz)
1100	1000	120
320	200	150
80	50	180

Table 1

4. Input impedance is a function of frequency. See Fig. 4.
5. The input can be operated down to DC but input slew rate must be better than 20V/µs.
6. All components should be suitable for the frequency in use.

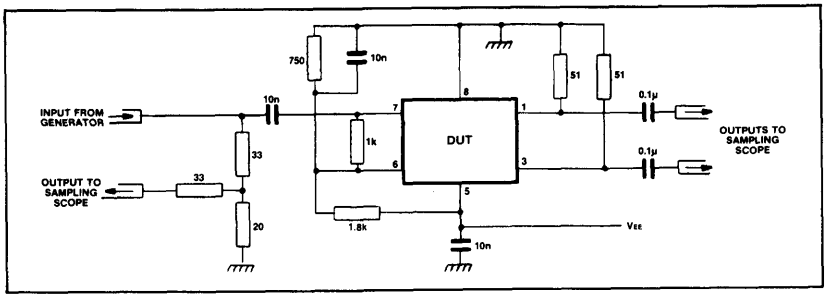


Fig.5 Test circuit

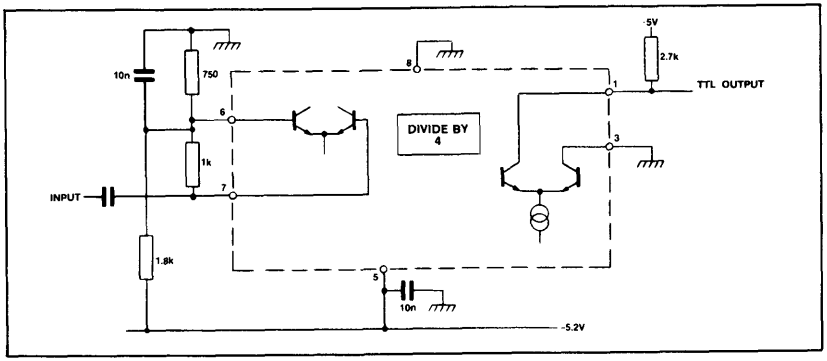


Fig.6 Typical application showing interfacing

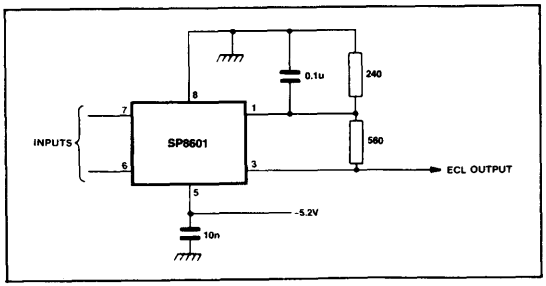


Fig.7 Interfacing to ECL

PLESSEY
Semiconductors

SP8602A & B 500MHz ÷ 2
SP8604A & B 300MHz ÷ 2

The SP8602 and SP8604 are emitter coupled logic dividers which feature ECL 10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

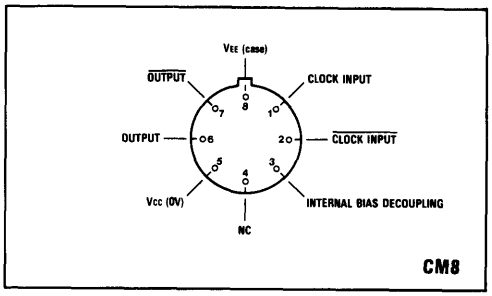


Fig.1 Pin connections - bottom view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 85mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 10mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

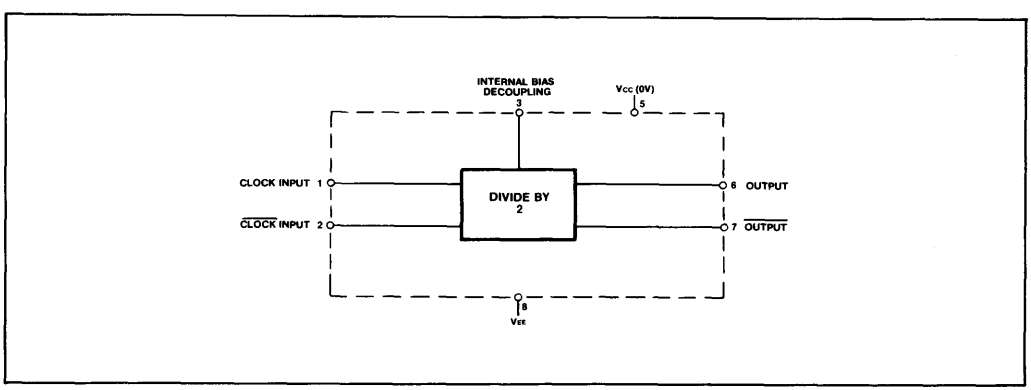


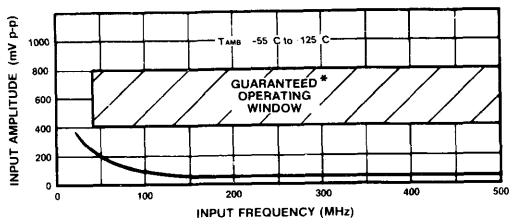
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} A Grade = -55°C to +125°C
B Grade = -30°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum frequency (sinewave input)	f_{max}	500		MHz	SP8602	Input = 400-800mV p-p	
		300		MHz	SP8604		
Minimum frequency (sinewave input)	f_{min}		40	MHz	All	Input = 400-800mV p-p	
Power supply current	I_{EE}		18	mA	All	V_{EE} = 5.2V Outputs unloaded	
Output low voltage	V_{OL}	-1.8	-1.4	V	All	V_{EE} = -5.2V	Note 4
Output high voltage	V_{OH}	-0.85	-0.7	V	All	V_{EE} = -5.2V	Note 4
Minimum output swing	V_{OUT}	400		mV	All	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.34mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified above.

Fig.3 Typical characteristic of SP8602A

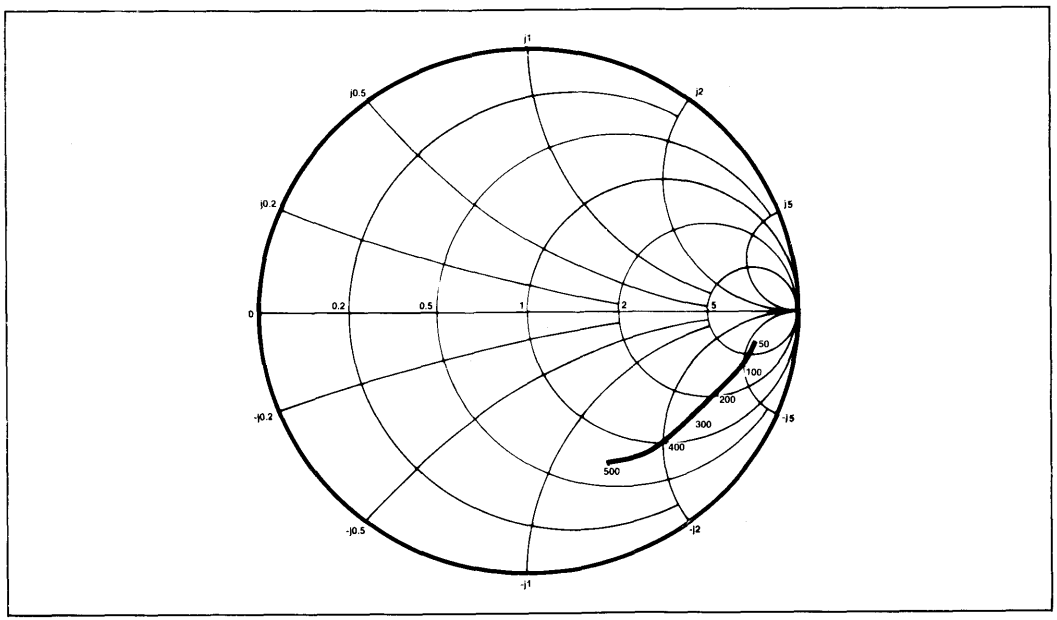


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 1 and 2) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the unused input to V_{EE} (ie pin 1 or 2 to pin 8). This causes a drop in sensitivity of about 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 4k on each output. The outputs can be interfaced to ECL 10K by addition of a pulldown resistor of 1.5k from the outputs to V_{EE} to increase output voltage swing.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

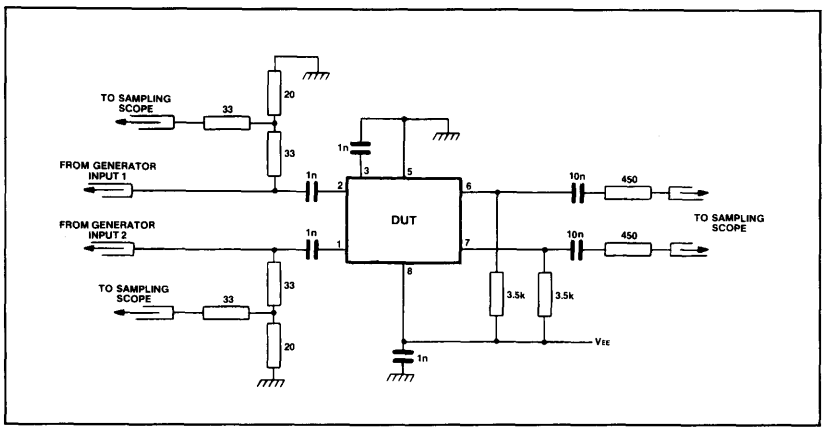


Fig.5 Test circuit

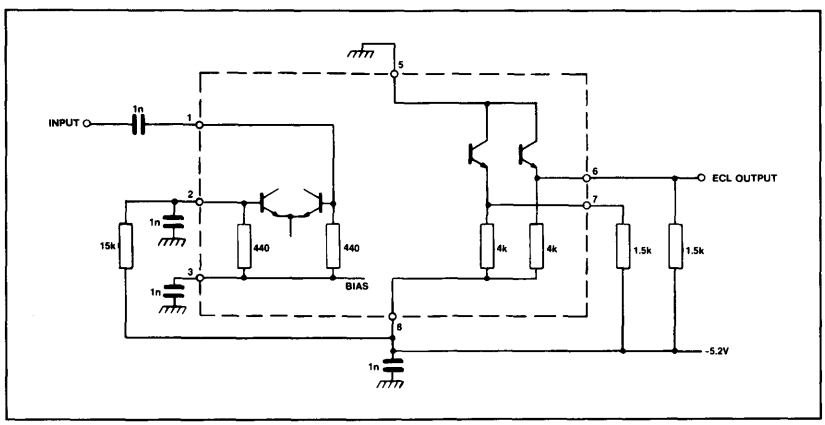


Fig.6 Typical application showing interfacing

PLESSEY
Semiconductors

SP8605A & B 1000MHz ÷ 2
SP8606A & B 1300MHz ÷ 2

The SP8605 and SP8606 are emitter coupled logic dividers with ECL III compatible outputs. Specified from -55°C to +125°C (A Grade), these devices feature AC coupled inputs and 600mV p-p clock input sensitivity.

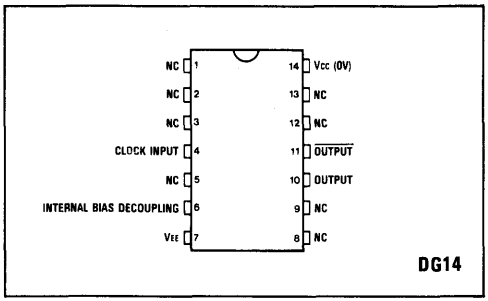


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 320mW
- Max. Input Frequency: 1300MHz (SP8606)
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - 0°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 10mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

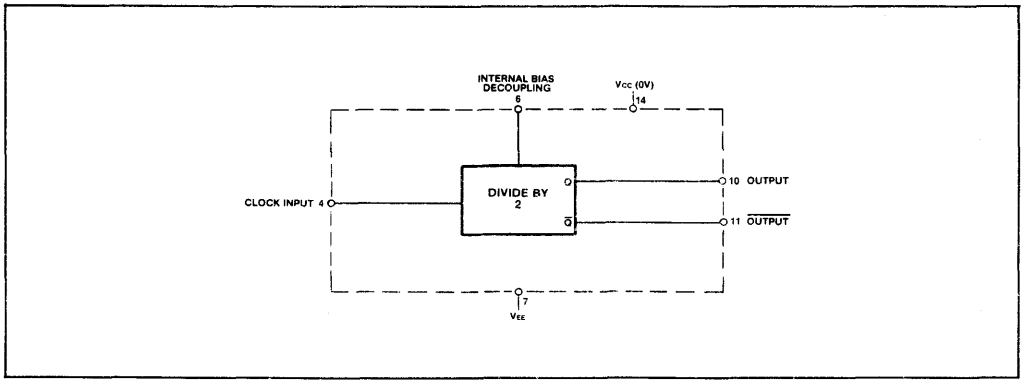


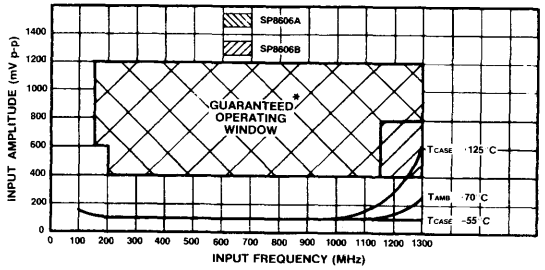
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{case} = -55°C to +125°C (Note 2)
B Grade T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum frequency (sinewave input)	f_{max}	1.0		GHz	SP8605A,B	Input = 400-1200mV p-p	Note 7
		1.3		GHz	SP8606A	Input = 800-1200mV p-p	Note 7
		1.3		GHz	SP8606B	Input = 400-1200mV p-p	Note 7
Minimum frequency (sinewave input)	f_{min}		150	MHz	All	Input = 600-1200mV p-p	Note 5
Current consumption	I_{EE}		100	mA	All	V_{EE} = -5.45V Outputs unloaded	Note 6
Output low voltage	V_{OL}	-1.92	-1.62	V	All	V_{EE} = -5.2V Outputs loaded with 430Ω(25°C)	
Output high voltage	V_{OH}	-0.93	-0.75	V	All	V_{EE} = -5.2V Outputs loaded with 430Ω(25°C)	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE} = -5.2V Outputs loaded with 430 ohms	Note 6

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The A grade devices must be used with a heat sink to maintain chip temperature below +175°C when operating in an ambient of +125°C.
3. The temperature coefficients of V_{OH} = +1.2mV/°C and V_{OL} = +0.24mV/°C but these are not tested.
4. The test configuration for dynamic testing is shown in Fig.5.
5. Tested at 25°C and +125°C only (+70°C for B grade).
6. Tested at 25°C only.
7. Tested at +125°C only (+70°C for B grade).



*Tested as specified above.

Fig.3 Typical characteristic of SP8606

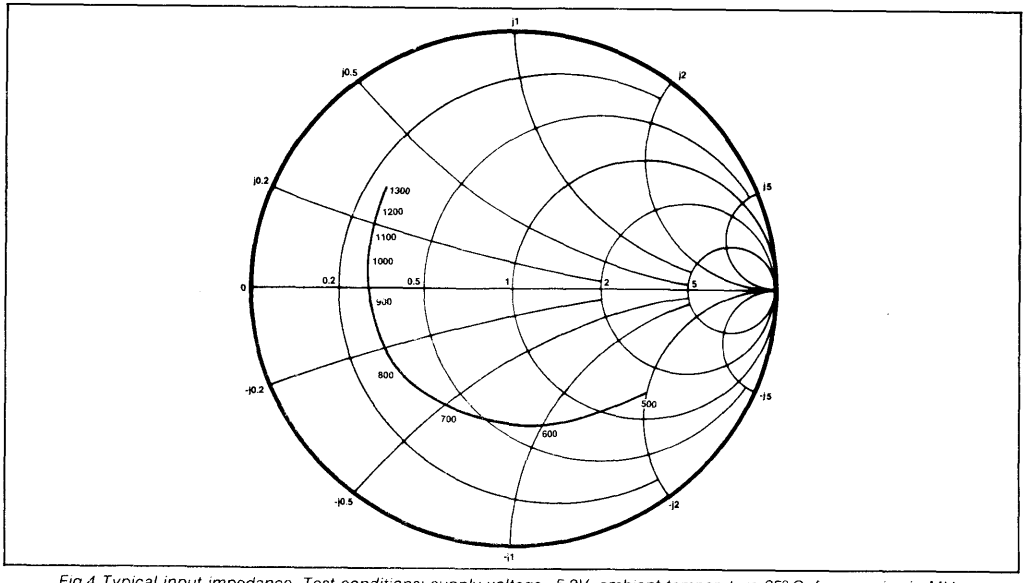


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 6, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the unused input to V_{EE} (ie pin 4 to pin 7). This reduces sensitivity by approximately 100mV.
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The input impedance of the SP8605/6 is a function of frequency. See Fig. 4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 ohms, and a value of 430 ohms is recommended. Interfacing to ECL III/10K is shown in Fig. 7.
6. These devices may be used with split supply lines and earth referenced input using the circuit shown in Fig. 6.
7. All components should be suitable for the frequency in use.

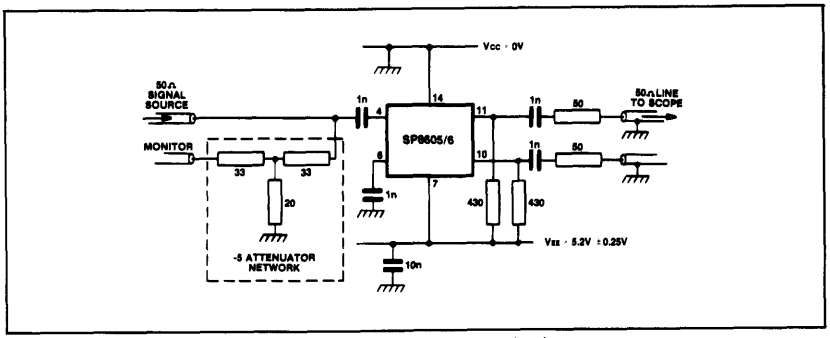


Fig.5 Toggle frequency test circuit

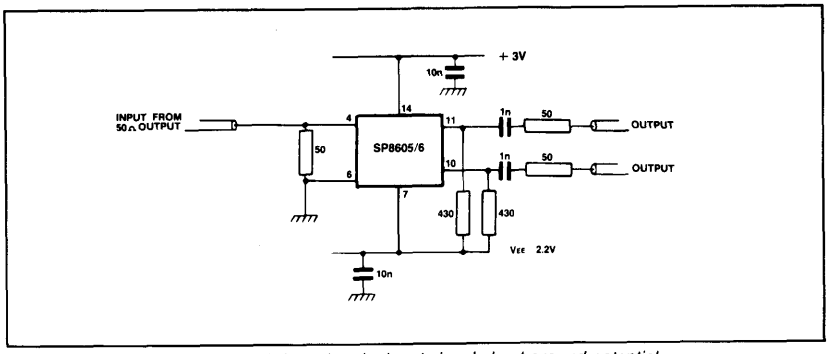


Fig.6 Circuit for using the input signal about ground potential

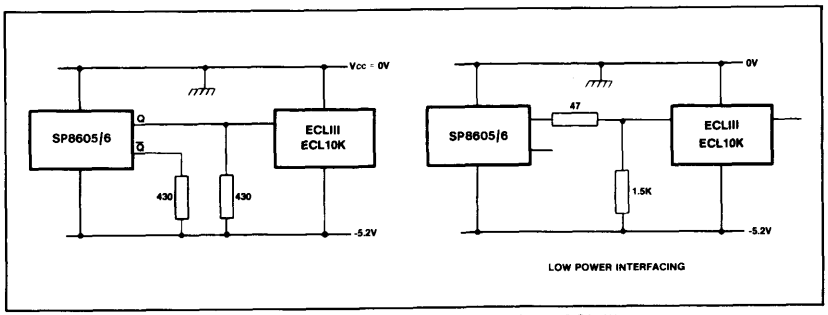


Fig.7 Interfacing SP8605/6 to ECL 10K and ECL III

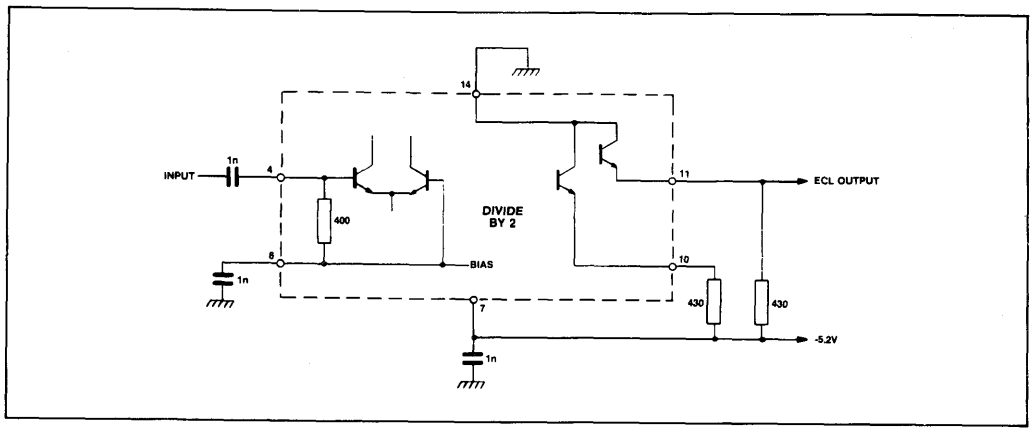


Fig.8 Typical application showing interfacing

PLESSEY
Semiconductors

SP8607A & B

600MHz ÷ 2

The SP8607 is an emitter coupled logic divider which features ECL 10K compatible outputs when used with external pulldown resistors. The inputs are AC coupled.

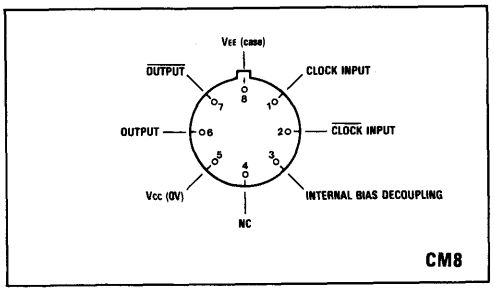


Fig.1 Pin connections - bottom view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 80mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 10mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

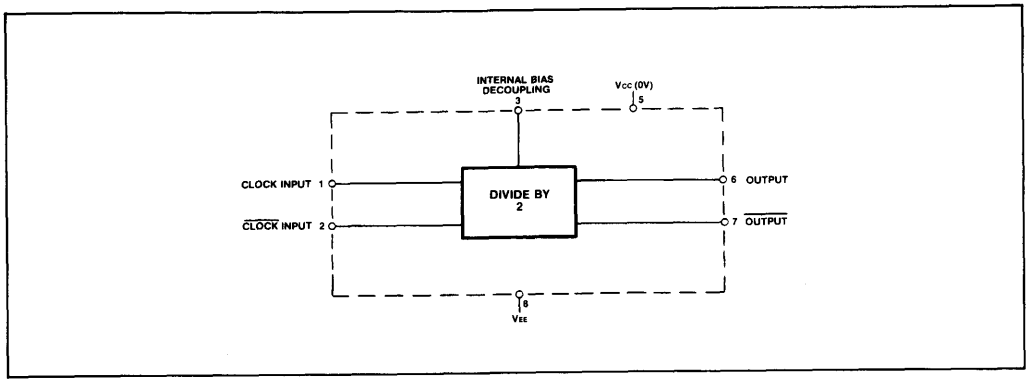


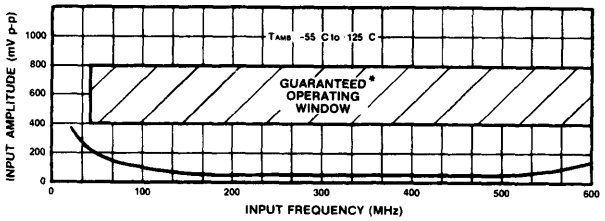
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} A Grade = -55°C to +125°C
B Grade = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		18	mA	V_{EE} = -5.2V Outputs unloaded	
Output low voltage	V_{OL}	-1.8	-1.4	V	V_{EE} = -5.2V	Note 4
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V	Note 4
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.34mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified above.

Fig.3 Typical characteristic of SP8607A

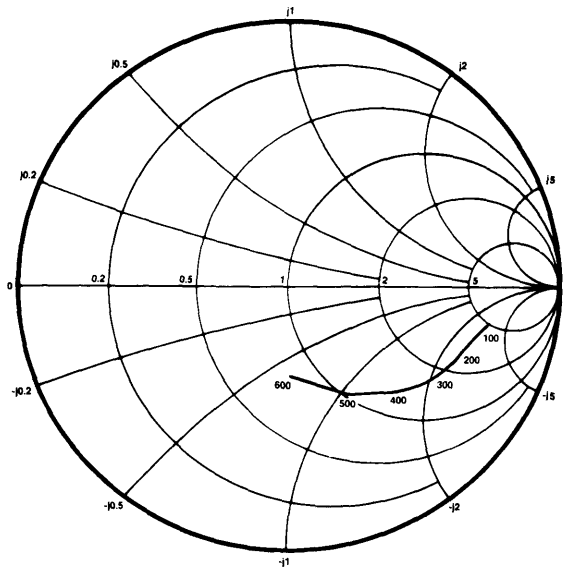


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 1 and 2) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 3, to ground.
2. In the absence of a signal the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the unused input to V_{EE} (ie pin 1 or 2 to pin 8). This causes a drop in sensitivity of about 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The outputs are compatible with ECL II. There is an internal load of 4k on each output. The outputs can be interfaced to ECL 10K by addition of a pulldown resistor of 1.5k to the outputs to increase the output voltage swing.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

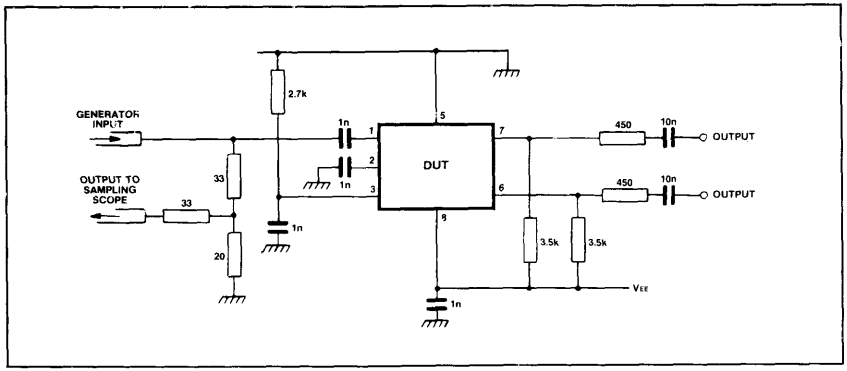


Fig.5 Test circuit

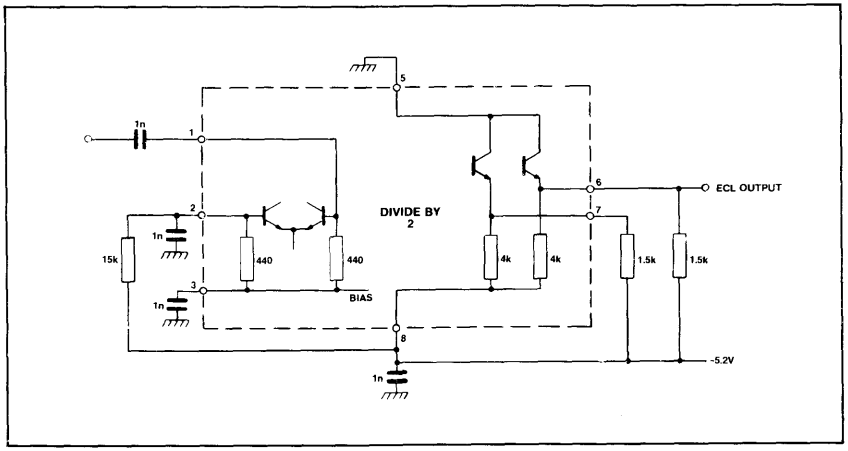


Fig.6 Typical application showing interfacing

PLESSEY
Semiconductors

SP8610A & B 1000MHz ÷ 4
SP8611A & B 1300/1500MHz ÷ 4

The SP8610/11 are asynchronous ECL divide by four circuits, with ECL compatible outputs which can also be used to drive 100 ohm lines. They feature input sensitivities of 600mV p-p (800mV p-p above 1300MHz).

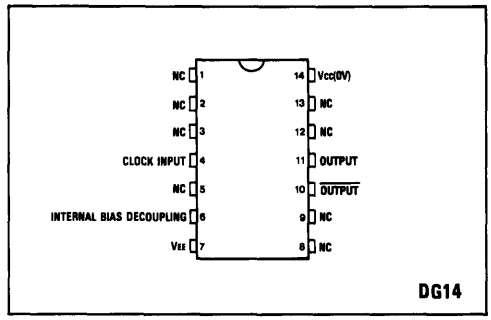


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Input (internal bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 380mW
- Max. Input Frequency: 1500MHz (SP8611B)
- Temperature Range:
  -55°C to +125°C (A Grade)
  0°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 10mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

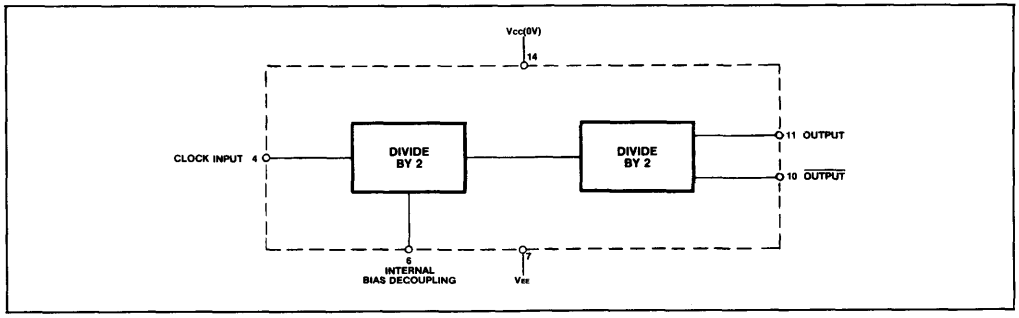


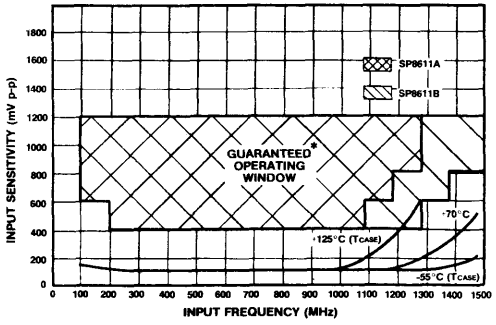
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{CASE} (A grade) = -55°C to +125°C (Note 2)
T_{amb} (B grade) = 0°C to +70°C

Characteristic	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Note
Maximum frequency	f_{max}	1.0		GHz	SP8610A,B	Input = 400-1200mV	Note 5
		1.3		GHz	SP8611A	Input = 800-1200mV	Note 7
		1.5		GHz	SP8611B	Input = 800-1200mV	Note 7
Minimum frequency	f_{min}		150	MHz	All	Input = 600-1200mV	Note 5
Current consumption	I_{EE}		100	mA	All	V_{EE} = -5.45V Outputs unloaded	Note 6
Output low voltage	V_{OL}	-1.92	-1.62	V	All	V_{EE} = -5.2V outputs loaded with 430Ω(25°C)	
Output high voltage	V_{OH}	-0.93	-0.75	V	All	V_{EE} = -5.2V outputs loaded with 430Ω(25°C)	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE} = -5.2V outputs loaded with 430Ω	Note 6

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The A grade devices must be used with a heat sink to maintain chip temperature below +175°C when operating in an ambient of +125°C.
3. The temperature coefficients of V_{OH} = +1.2mV/°C and V_{OL} = +0.24mV/°C but these are not tested.
4. The test configuration for dynamic testing is shown in Fig.5.
5. Tested at 25°C and +125°C only (+70°C for B grade).
6. Tested at 25°C only.
7. Tested at +125°C only (+70°C for B grade).



*Tested as specified above.

Fig.3 Typical input characteristics

OPERATING NOTES

1. The clock input (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 6 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the input to V_{EE} (i.e. Pin 4 to Pin 7). This reduces sensitivity by approximately 100mV.
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The input impedance of the SP8610/11 is a function of frequency. See Fig. 4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 ohms, and a value of 430 ohms is recommended. Interfacing to ECL III/10K is shown in Fig. 7.
6. These devices may be used with split supply lines and ground referenced input by means of the circuit of Fig. 6.

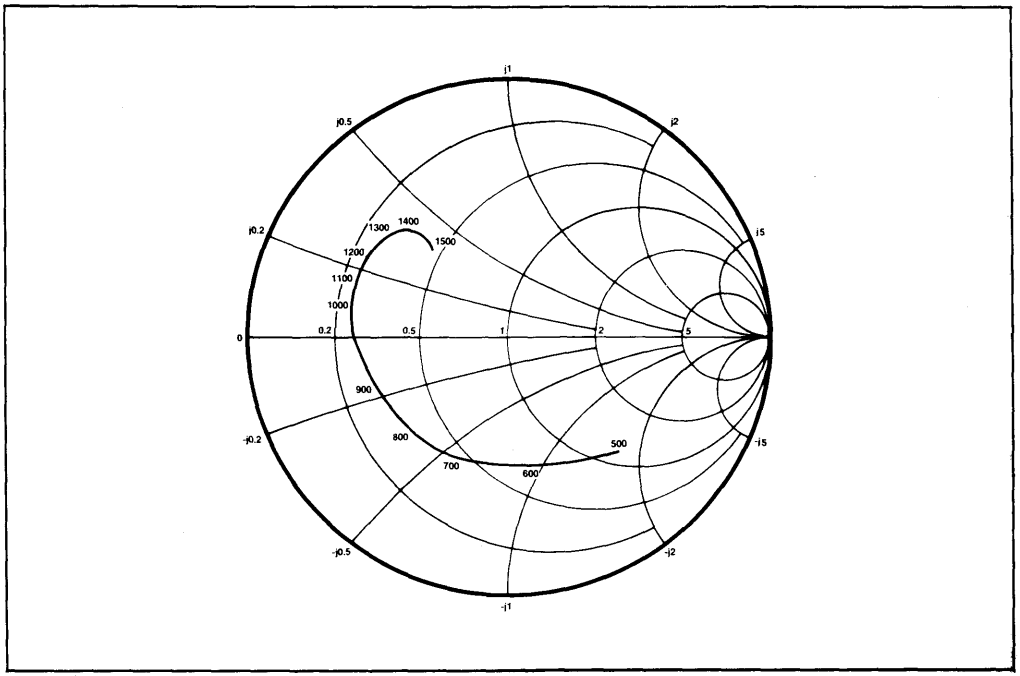


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

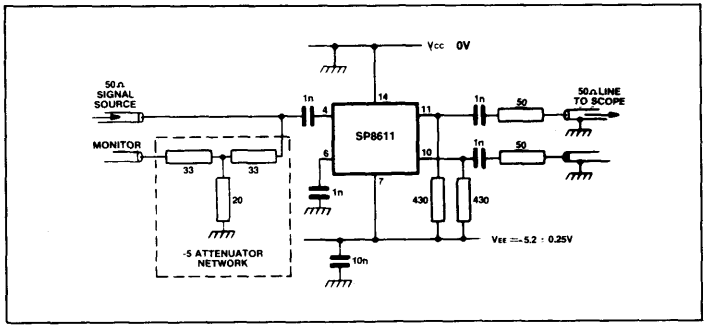


Fig.5 Toggle frequency test circuit

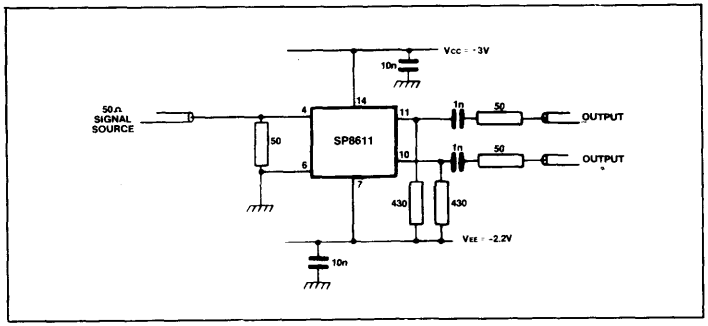


Fig.6 Circuit for using the input signal about earth potential

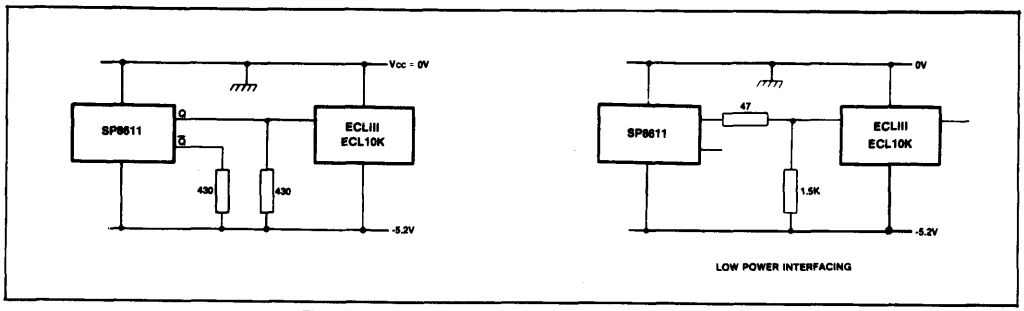


Fig.7 Interfacing SP8611 series to ECL 10K and ECL III

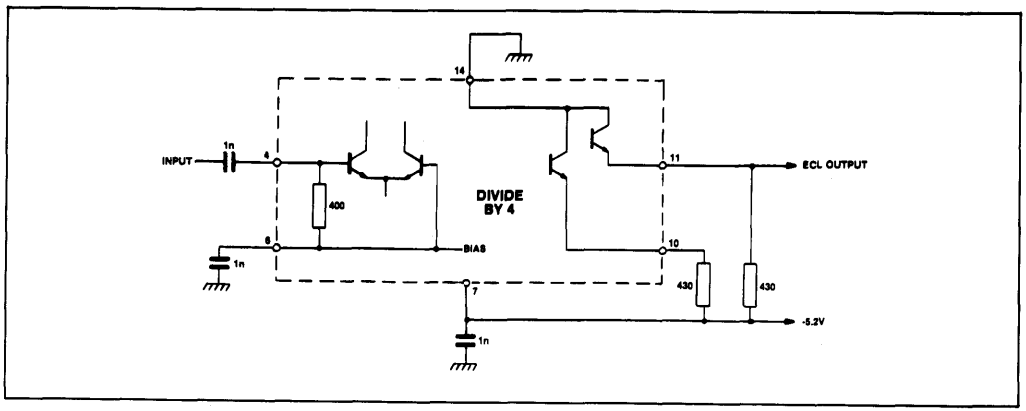


Fig.8 Typical application showing interfacing

PLESSEY
Semiconductors

SP8612B

1800MHz ÷ 4

The SP8612B is an asynchronous emitter coupled logic counter which provides ECL 10K compatible outputs and can drive 100 ohm lines. It operates from a -6.8V supply or split supplies of +5V and -1.8V. Otherwise it is similar to the SP8610/11.

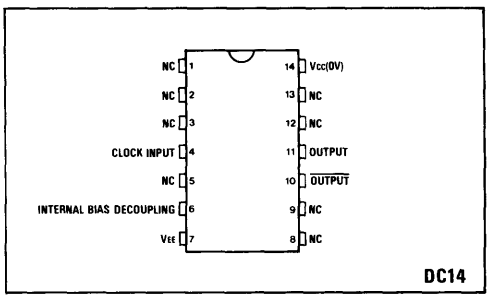


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Input (Internal Bias)
- Typical Operating Frequency 2GHz

QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 600mW
- Output Voltage Swing: 750mV typ.

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: (V_{CC}-V_{EE}) -8V
- Output Current: 15mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Input Voltage: 2.5V p-p

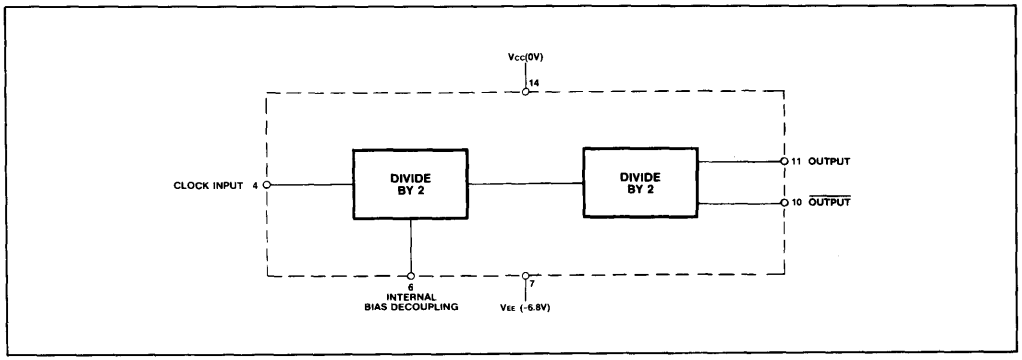


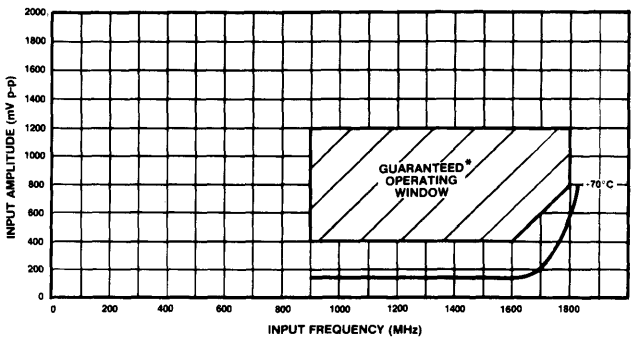
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -6.8V ± 0.35V
Temperature: T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Note
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	1.8		GHz	Input = 800-1200mV p-p	Note 4
Minimum frequency sinewave input	f_{min}		900	MHz	Input = 400-1200mV p-p	Note 5
Power supply current	I_{EE}		110	mA	Outputs unloaded V_{EE} = -7.15V	Note 5
Output low voltage	V_{OL}	-1.9	-1.62	V	Outputs loaded with 620Ω to V_{EE} = -6.8V(25°C)	
Output high voltage	V_{OH}	-0.93	-0.75	V	Outputs loaded with 620Ω to V_{EE} = -6.8V(25°C)	
Minimum output swing	V_{OUT}	500		mV	Outputs loaded with 620Ω to V_{EE} = -6.8V	Note 5

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.2mV/°C and V_{OL} = +0.24mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at +70°C only.
5. Tested at 25°C only.



* Tested as specified above.

Fig.3 Typical input characteristics SP8612B

OPERATING NOTES

1. The clock input (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 6 to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the input to V_{EE} (i.e. pin 4 to pin 7). This reduces sensitivity by approximately 100mV.
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The input impedance of the SP8612 is a function of frequency. See Fig. 4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 ohms, and a value of 620 ohms is recommended. Interfacing to ECL III/10K is shown in Fig. 7.
6. These devices may be used with split supply lines by means of the circuit of Fig. 6. Some improvement in the upper frequency of operation may be obtained under these conditions, but suitable circuit layout must be employed to achieve this improvement.

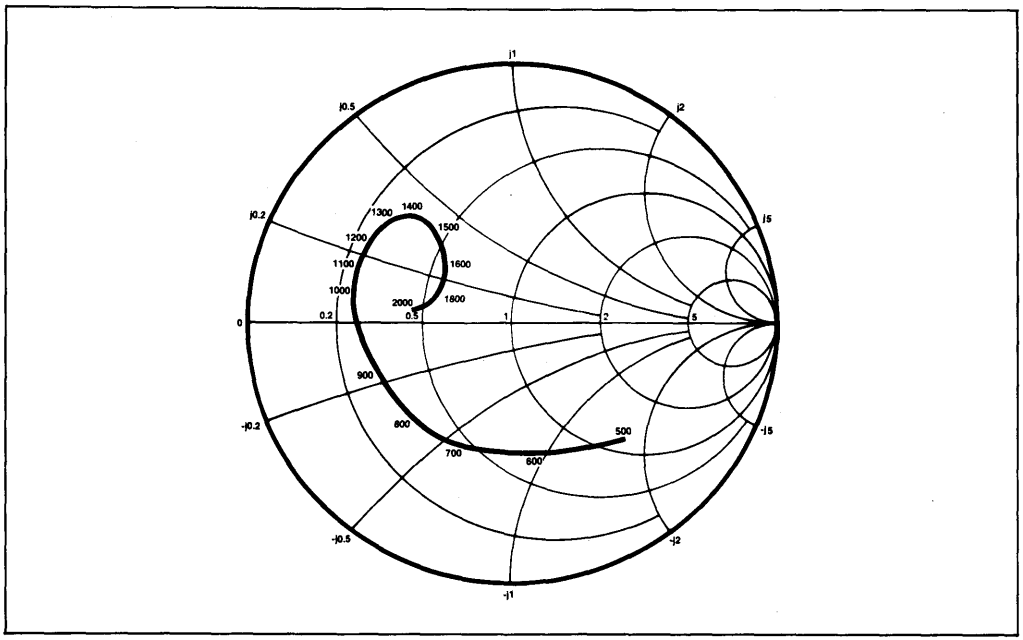


Fig.4 Typical input impedance. Test conditions: supply voltage -6.8V ambient temperature 25° C. Frequencies in MHz, impedances normalised to 50 ohms.

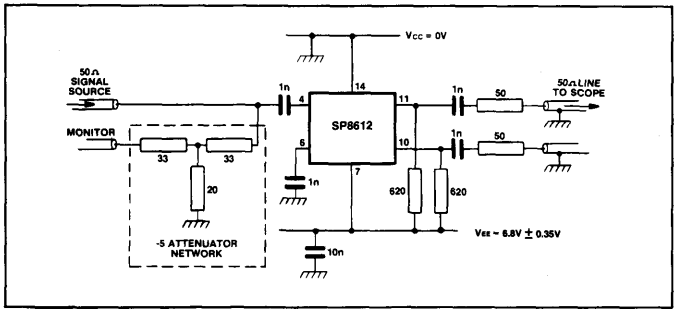


Fig.5 Toggle frequency test circuit

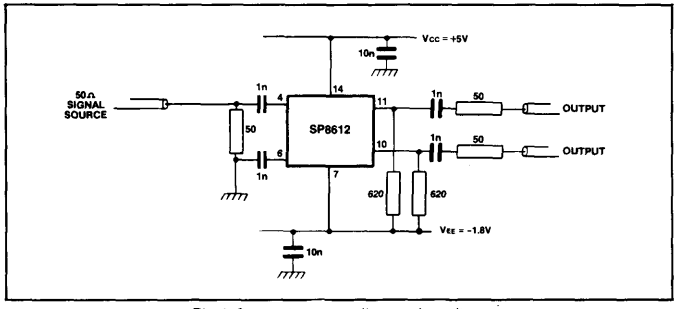


Fig.6 Operation on split supply voltages

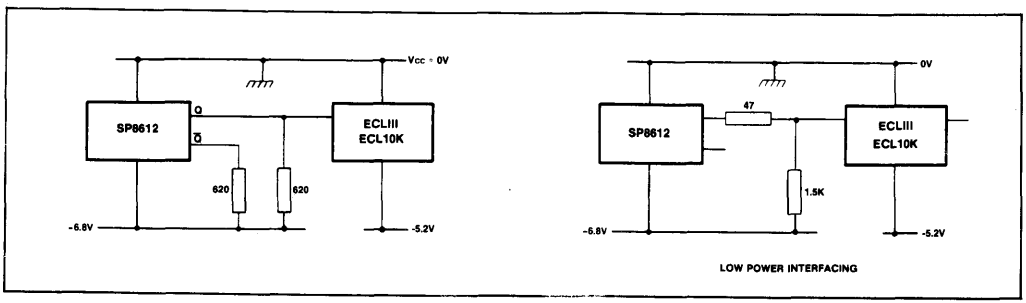


Fig.7 Interfacing SP8612 series to ECL 10K and ECL III

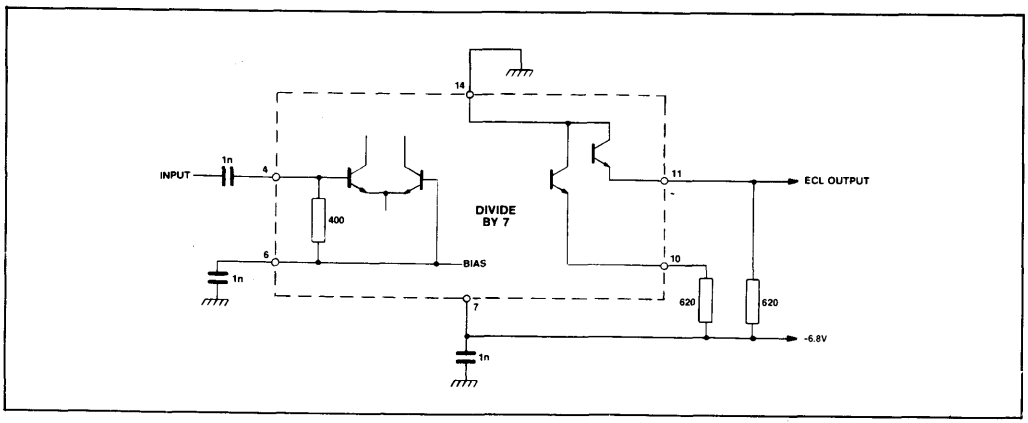


Fig.8 Typical application showing interfacing

PLESSEY
Semiconductors

SP8620A & B

400MHz ÷ 5

The SP8620 is an asynchronous emitter coupled logic counter which provides ECL compatible outputs when external pulldown resistors are added. It requires an AC coupled input of 600mV p-p.

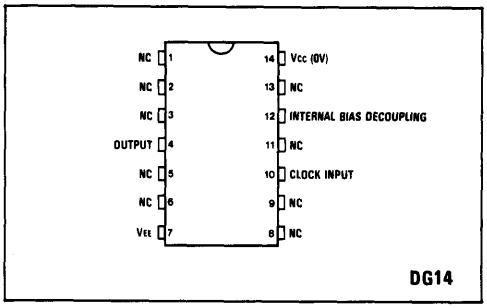


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 285mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 15mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

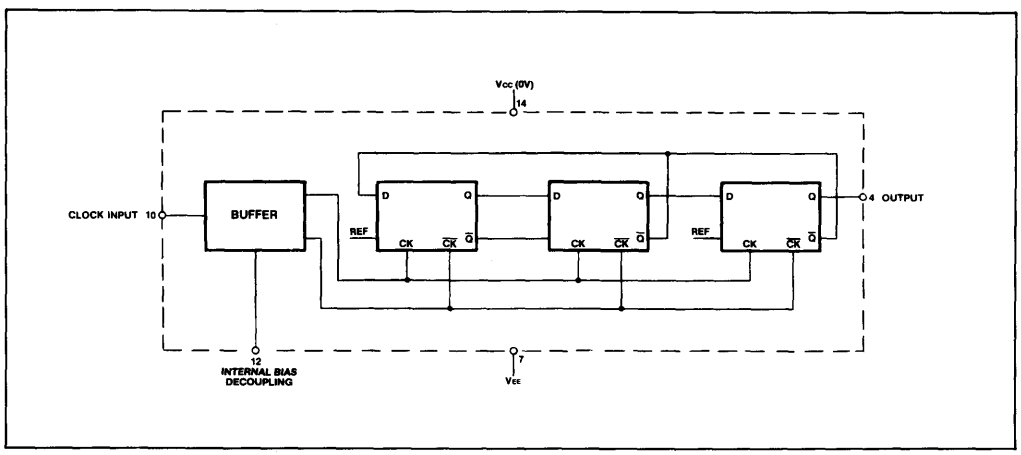


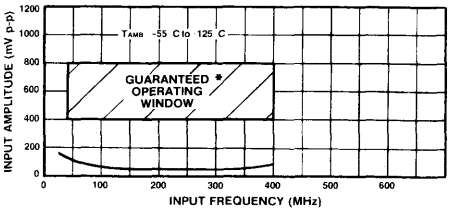
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Conditions	Note
Maximum frequency (sinewave input)	f_{max}	400		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		55	mA	V_{EE} = -5.2V	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified above.

Fig.3 Typical input characteristic of SP8620A

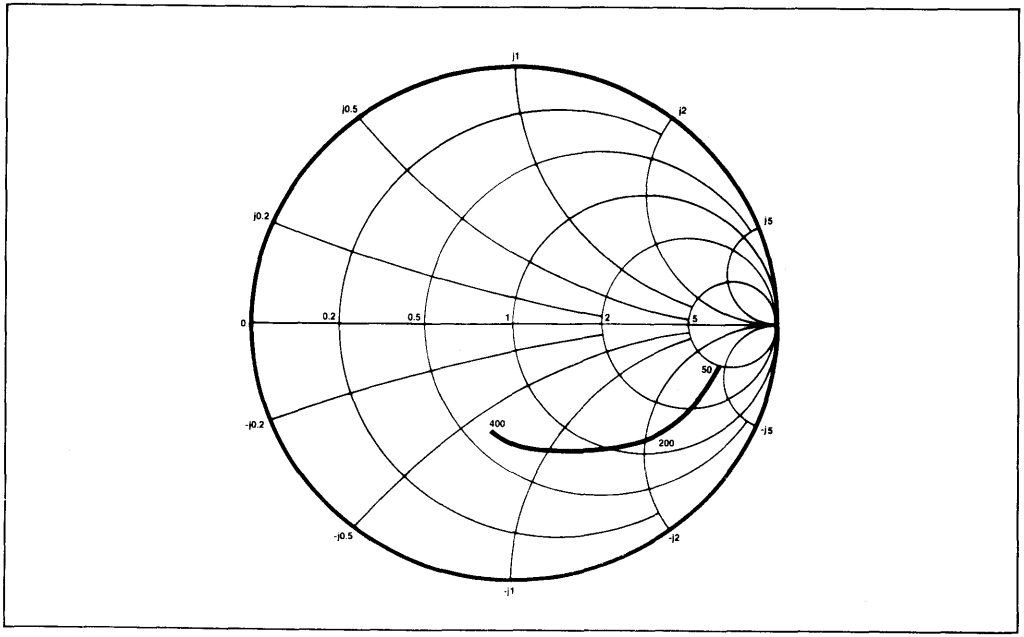


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the clock input to V_{EE} (ie Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 3k at the output. The output can be interfaced to ECL/10K by the addition of 1.5k to the output to increase the output voltage swing.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

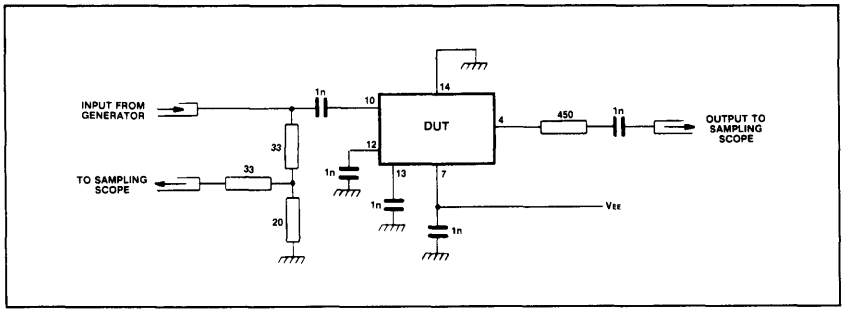


Fig.5 Test circuit

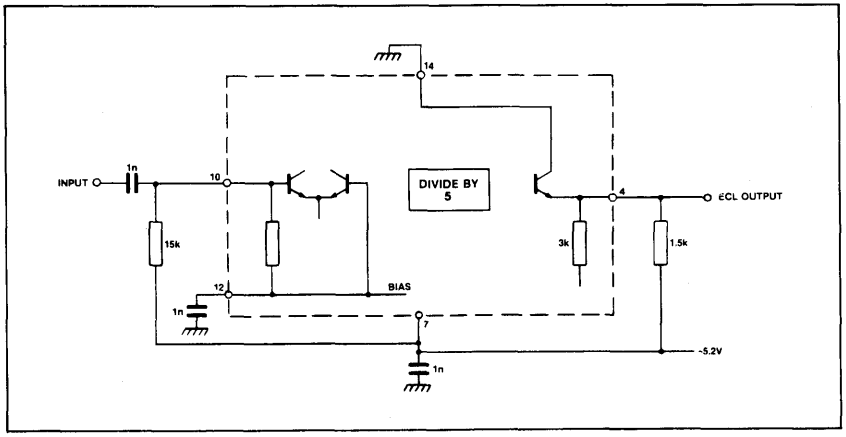


Fig.6 Typical application showing interfacing

PLESSEY
Semiconductors

SP8629

150MHz ÷ 100

The SP8629 is an ECL counter which provides a TTL compatible output, high input sensitivity and low power consumption. Pin compatible with DM8629, it features a much lower power consumption.

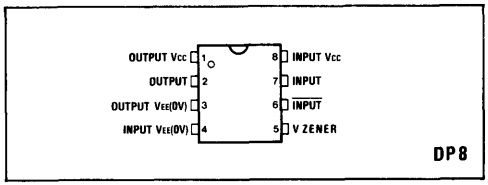


Fig.1 Pin connections - top view

FEATURES

- TTL/CMOS Compatible Output
- High Input Sensitivity
- Ideal Frequency Counter Prescaler
- On Chip Zener Diode

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 170mW
- Temperature Range: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage (Pins 1 and 8): 8V
- Output Current: 40mA
- Storage Temperature Range: -30°C to +85°C
- Max. Junction Temperature: +175°C
- Input Voltage: 2.5V p-p

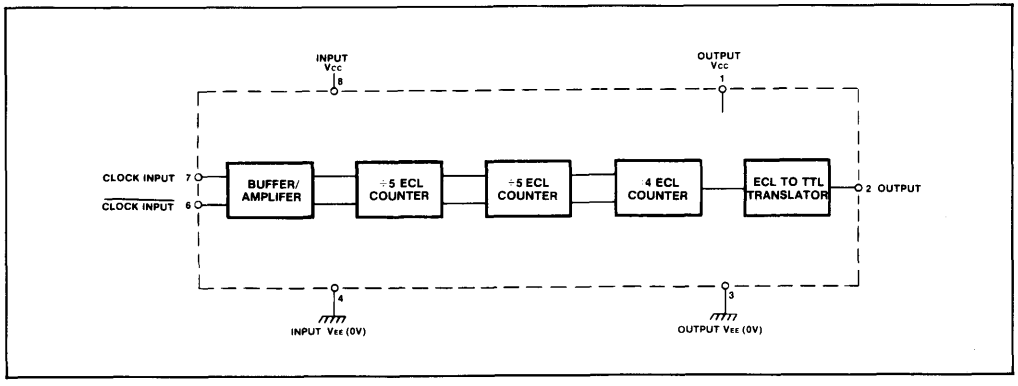


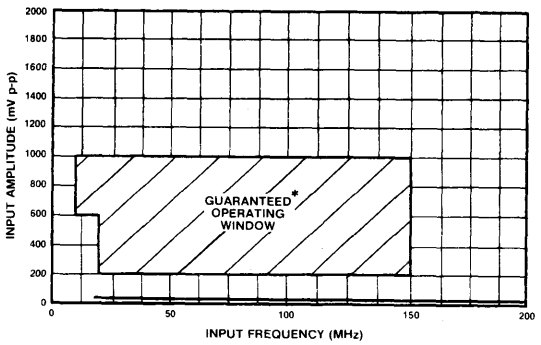
Fig.2 SP8629 logic diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ±0.52V V_{EE} = 0V
Temperature: T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum toggle frequency sinewave input	f_{max}	150		MHz	Input = 200-1000mV p-p
Minimum toggle frequency sinewave input	f_{min}		10	MHz	Input = 600-1000mV p-p
Power supply current	I_{EE}		45	mA	
Output high voltage	V_{OH}	2.4		V	V_{CC} = 4.68V I_{OH} = -400µA
Output high voltage	V_{OH}	2.0		V	V_{CC} = 4.68V I_{OH} -1.6mA
Output low voltage	V_{OL}		0.5	V	V_{CC} = 5.72V I_{OL} 8mA
Output short circuit current	I_{OS}	-10	-40	mA	V_{CC} = 5.72V
Internal zener voltage	V_Z	5.85	6.65	V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. All characteristics above are tested at 25°C only.



*Tested as specified above.

Fig.3 Typical input characteristics SP8629

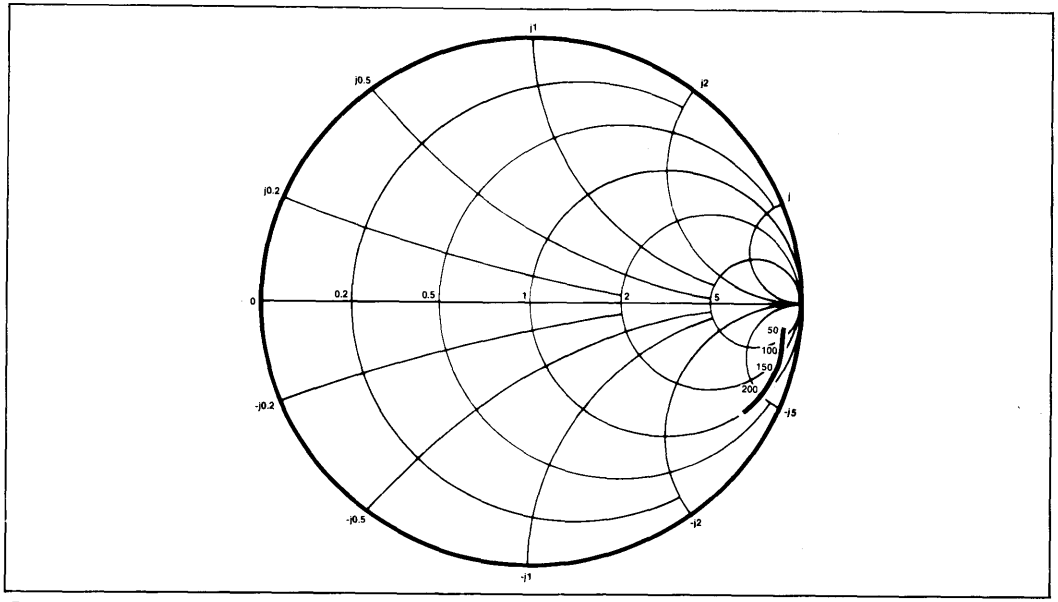


Fig.4 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25°C. Frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. Two V_{EE} and two V_{CC} connections are provided, separating the ECL stages from the TTL section, isolating the noise transients inherent in the TTL structure. In most cases, shorting the two V_{EE} pins to a good ground plane and the V_{CC} pins to a wide V_{CC} bus will provide sufficient isolation. All components used in the circuit layout should be suitable for the frequencies involved and leads should be kept short to minimise stray inductance.
2. The signal source is usually capacitively coupled to the input as shown in Fig. 6. In the single-ended mode a capacitor of 0.01µF (C2) should be connected between the unused input and the ground plane to provide a good high frequency bypass. The capacitor should be increased at lower frequencies. If the input is likely to be interrupted, it may be desirable to connect a 100k resistor between an input and ground.
3. In the single ended mode it is preferable to connect the resistor to the unused input. The addition of the 100k resistor causes a loss of input sensitivity, but prevents circuit oscillations under no signal (open circuit) conditions.
4. The input waveform will normally be sinusoidal but below 10MHz correct operation depends on the slew rate of the input signal. A slew rate of 50V/µs will enable the device to operate down to DC. The device will operate with a TTL input signal as shown in Fig. 7 and is DC coupled to the input.

The device can be used in phase locked loop applications such as FM radio or other communications bands to prescale the input frequency down to a more useable level. A digital frequency display system can also be derived separately or in conjunction with a phase locked loop, and it can extend the useful range of many inexpensive frequency counters to, typically, 200MHz.
5. The on-chip Zener diode allows a simple stabilised power supply to be constructed with the addition of a few extra external components, as shown in Fig. 8, to the SP8629.
6. The INPUT is positive edge triggered while the $\overline{\text{INPUT}}$ triggers on the negative edge.

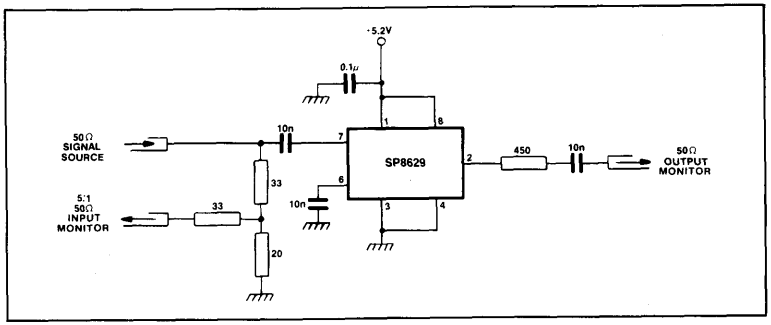


Fig.5 Test circuit

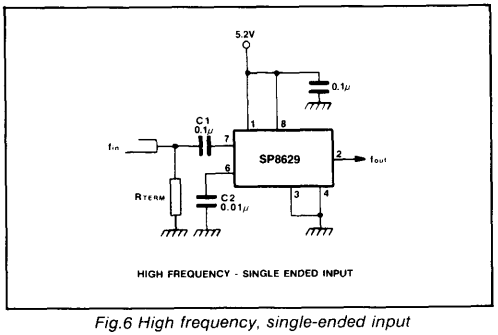


Fig.6 High frequency, single-ended input

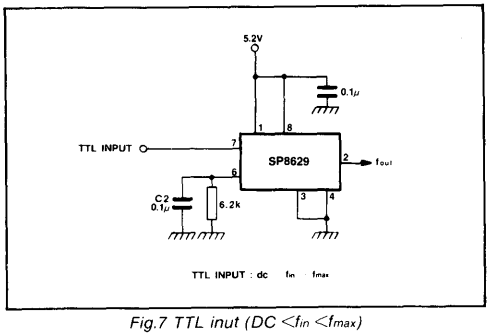


Fig.7 TTL inut (DC <f_{in} <f_{max})

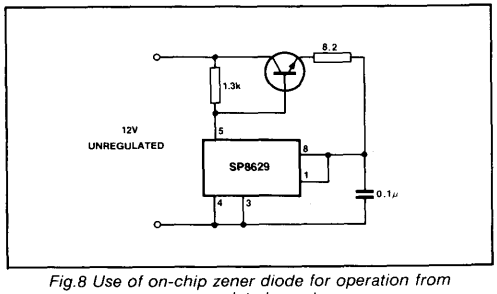


Fig.8 Use of on-chip zener diode for operation from unregulated supply

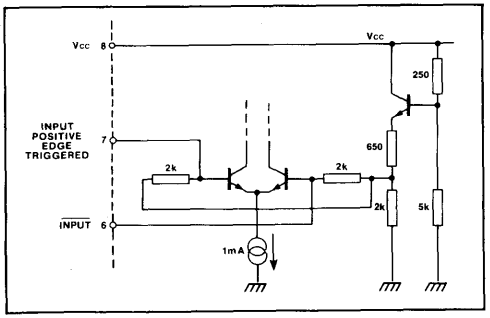


Fig.9 Input circuit diagram

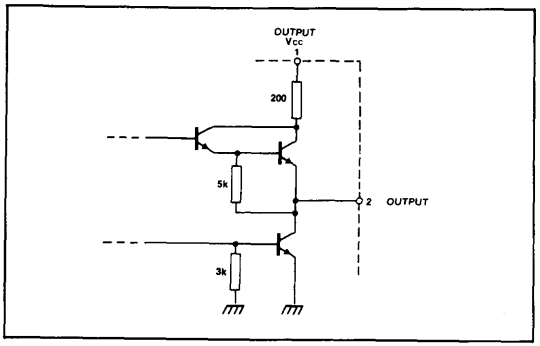


Fig.10 Output circuit diagram

PLESSEY
Semiconductors

SP8630A & B

600MHz ÷ 10

The SP8630 is an asynchronous emitter coupled logic counter which provides ECL compatible outputs when used with external pulldown resistors. It requires an AC coupled input of 600mV p-p.

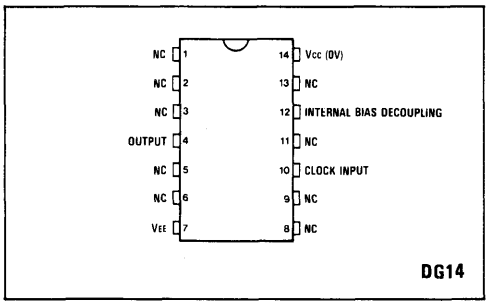


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 350mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 15mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

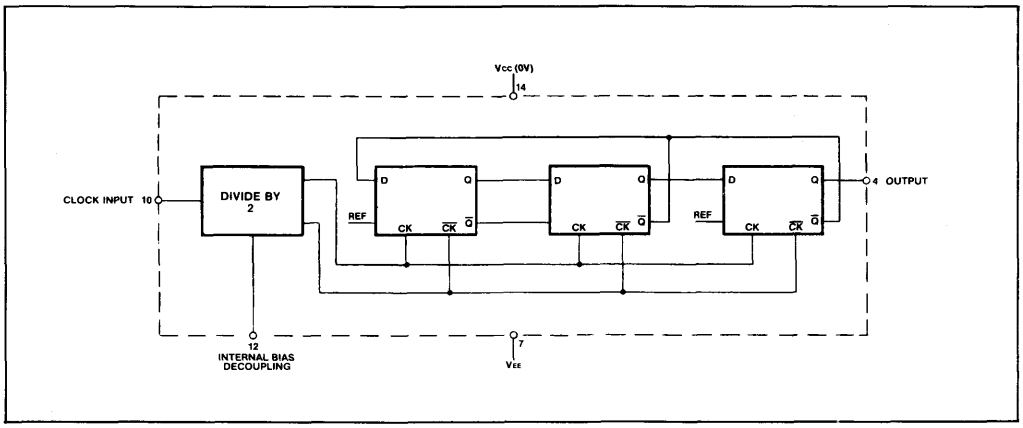


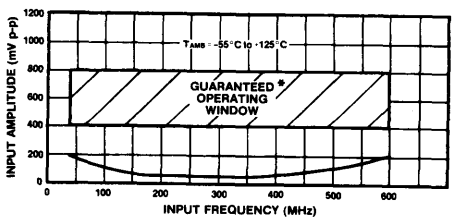
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Note
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		70	mA	V_{EE} = -5.2V	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
Minimum output swing	V_{OUT}	400		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



* Tested as specified above.

Fig.3 Typical input characteristic of SP8630A

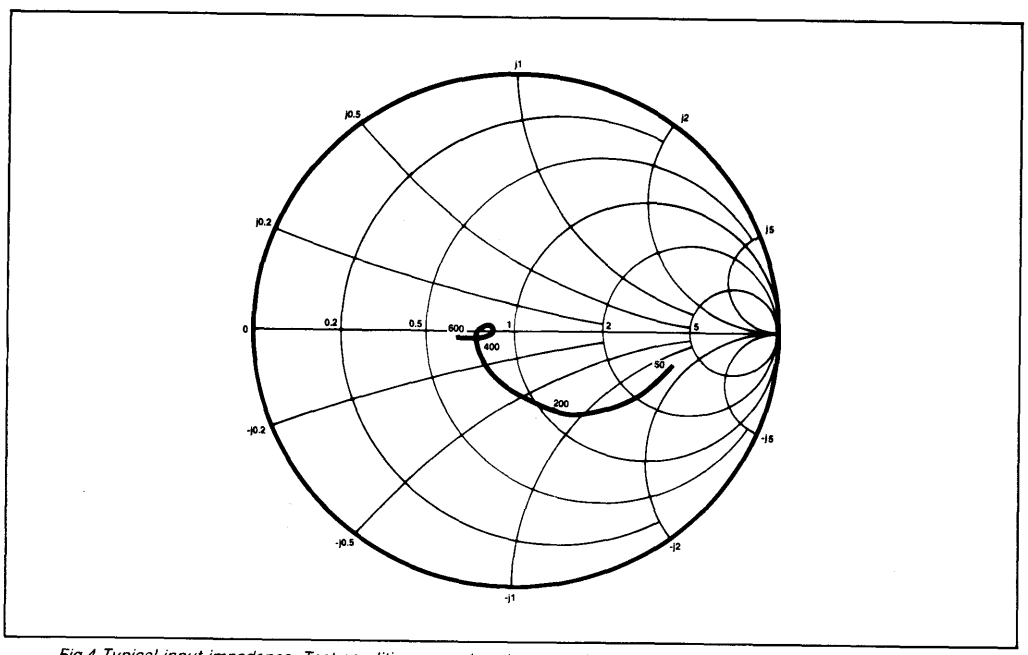


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (ie Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 3k at output. The output can be interfaced to ECL/10K by the addition of 1.5k to the output to increase the output voltage swing.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

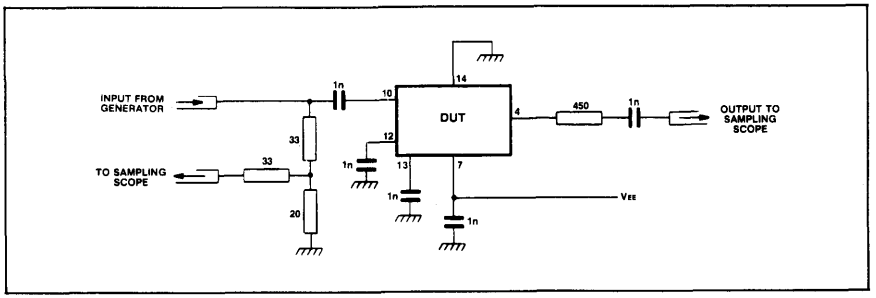


Fig.5 Test circuit

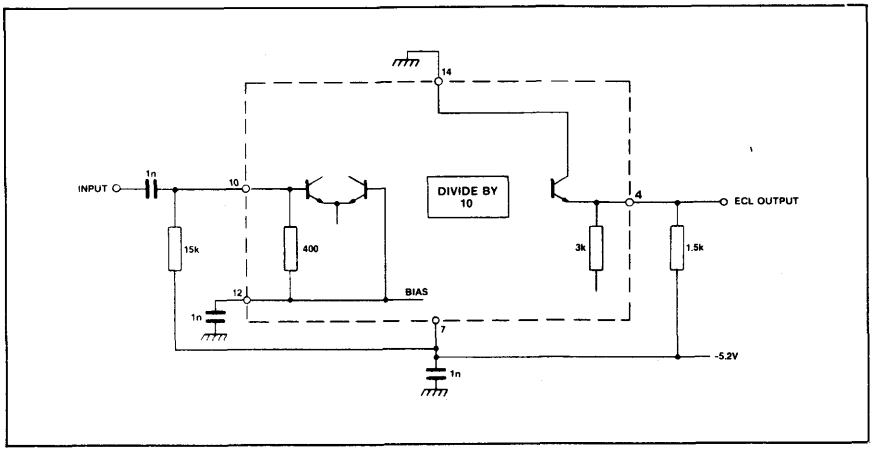


Fig.6 Typical application showing interfacing

PLESSEY
Semiconductors

SP8634B SP8635B SP8637B

700/600/400MHz ÷ 10 (BCD OUTPUTS)

The SP8634/5 and 7 are ECL decade counters with TTL compatible BCD outputs. They require an AC coupled input of 600mV p-p and have an ECL 10K compatible inhibit input which inhibits the device when in the high state. Both ECL and TTL 'carry' outputs are provided and there is a TTL reset.

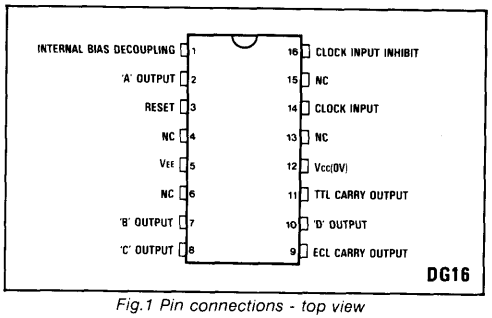


Fig.1 Pin connections - top view

FEATURES

- BCD Outputs TTL Compatible
- Reset Input TTL Compatible
- AC Coupled Input (Internal Bias)
- TTL and ECL Compatible Carry Outputs
- Clock Inhibit Input ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.2V
- Power Consumption: 400mW
- Temperature Range: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- BCD Outputs Voltage: V_{EE} +11V
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Input Voltage: 2.5V p-p

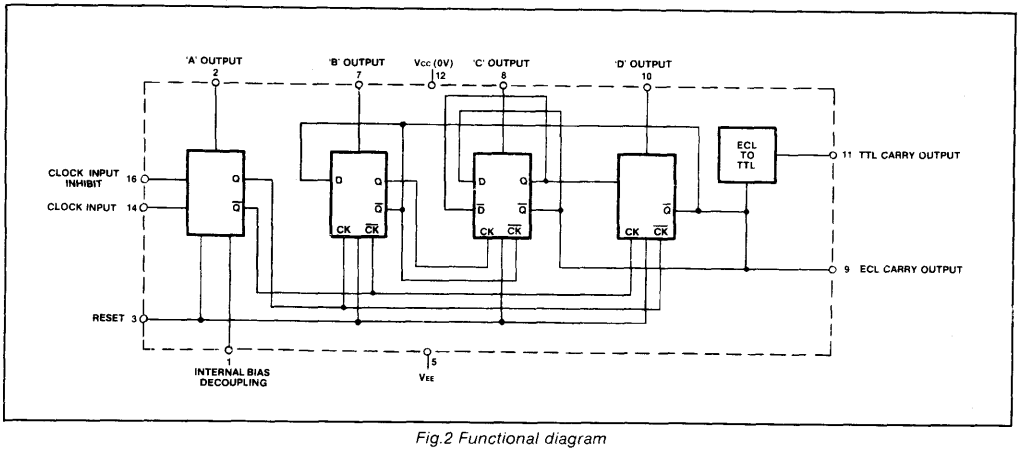


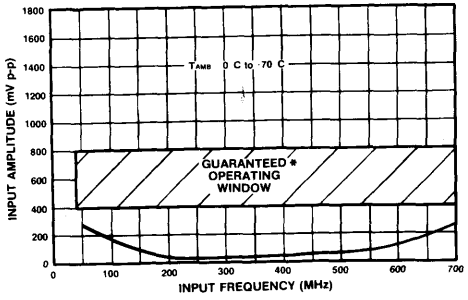
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Notes
Maximum frequency sinewave input	f_{max}	700		MHz	SP8634B	Input = 400-800mV p-p	Note 5
		600		MHz	SP8635B		
		400		MHz	SP8637B		
Minimum frequency sinewave input	f_{min}		40	MHz	All	Input = 400-800mV p-p	Note 7
Power supply current	I_{EE}		90	mA	All	V_{EE} = -5.2V	Note 6
Clock inhibit high voltage	V_{INH}	-0.96		V	All	V_{EE} = -5.2V (25°C)	
Clock inhibit low voltage	V_{INL}		-1.65	V	All	V_{EE} = -5.2V (25°C)	
TTL output high voltage (pin 2,7,8,10)	V_{OH}	2.4		V	All	10kΩ from TTL output too +5V	Note 6
TTL output low voltage (pin 2,7,8,10)	V_{OL}		0.4	V	All	10kΩ from TTL output to +5V	Note 6
TTL output voltage (pin 11)	V_{OH}	2.4		V	All	5kΩ from TTL output to +5V	Note 6
TTL output low voltage (pin 11)	V_{OL}		0.4	V	All	5kΩ from TTL output to +5V	Note 6
ECL output high voltage (pin 9)	V_{OH}	-0.9	-0.7	V	All	V_{EE} = -5.2V (25°C)	
ECL output low voltage (pin 9)	V_{OL}	-1.8	-1.5	V	All	V_{EE} = -5.2V (25°C)	
Edge speed for correct operation at maximum frequency	t_E		2.5	ns	All	10% to 90%	Note 7
Reset on time for correct operation	t_{ON}	100		ns	All		Note 7
Reset input high voltage	V_{INH}	2.4		V	All		Note 6
Reset input low voltage	V_{INL}		0.5	V	All		Note 6

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} (ECL) = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
3. The temperature coefficient of inhibit threshold voltage = +0.24mV/°C but this is not tested.
4. The test configuration for dynamic testing is shown in Fig.5.
5. Tested at 0°C and +70°C only.
6. Tested at +25°C only.
7. Guaranteed but not tested.



* Tested as specified above.

Fig.3 Typical input characteristics SP8634

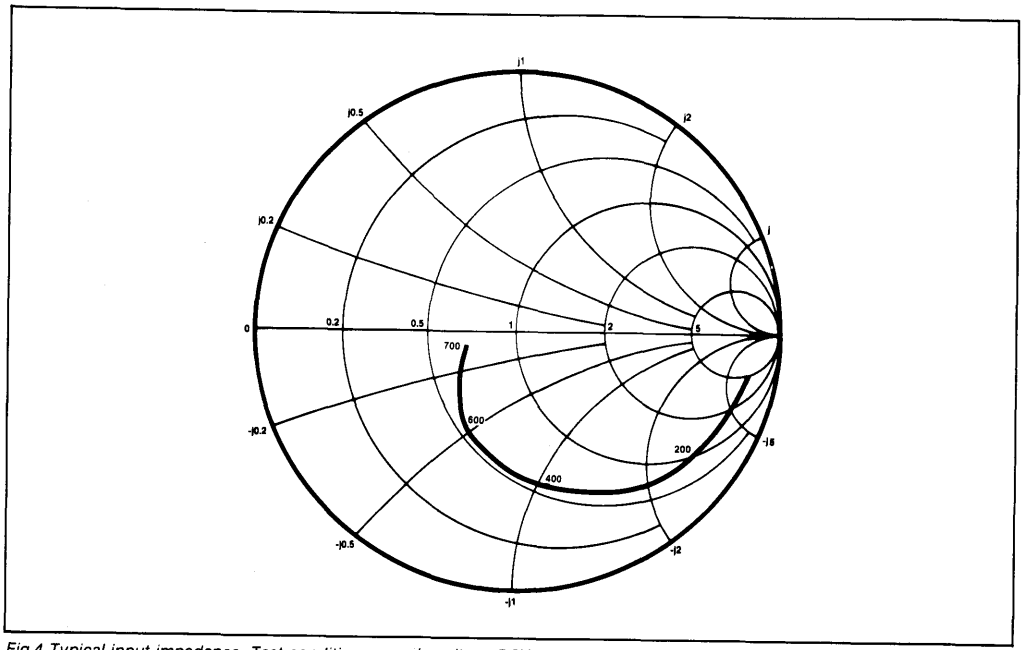


Fig.4 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C. Frequencies in MHz, impedances normalised to 50 ohms.

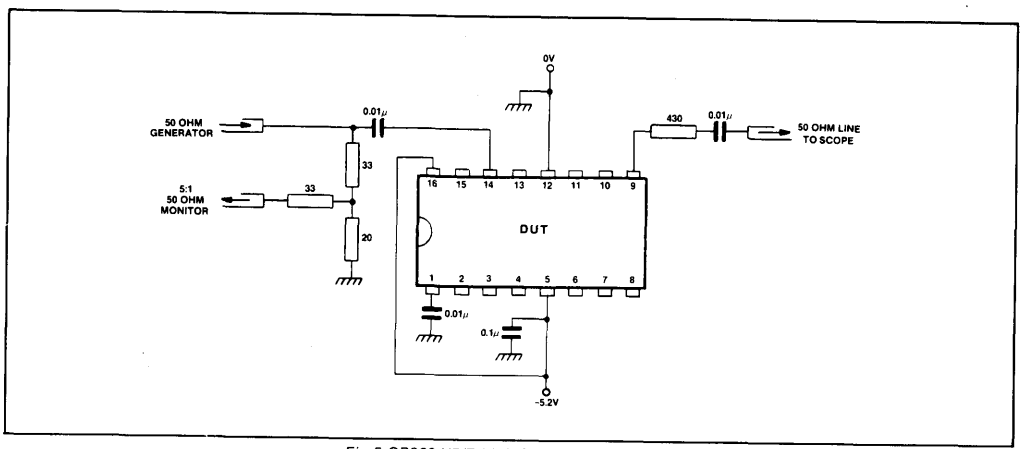


Fig.5 SP8634/5/7 high frequency test circuit

OPERATING NOTES

1. The clock input (pin 14) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 1, to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 68k resistor between the clock input, pin 14, and the negative supply (pin 5).
3. The device will operate down to DC but the input slew rate must be better than 100V/μs.
4. The Carry O/P is ECL II compatible but can be interfaced ECL III/10K by the inclusion of two resistors. See Fig. 7.
5. The clock inhibit is compatible with ECL III/10K throughout the temperature range.
6. The output (pins 2, 7, 8, 10 and 11) are current sources and can be made TTL compatible by addition of 10k and 5k (pin 11) to +5V. See Fig.6. This gives a fan-out of 1. This can be increased by buffering the output with a PNP emitter follower. See Fig.8.
7. The device is clocked on the positive transition of the clock input on pin 14, provided that the clock inhibit input (pin 16) is in the low state. It is important to note that the positive transition of clock inhibit must occur while the clock is in the high state to avoid spurious counting.

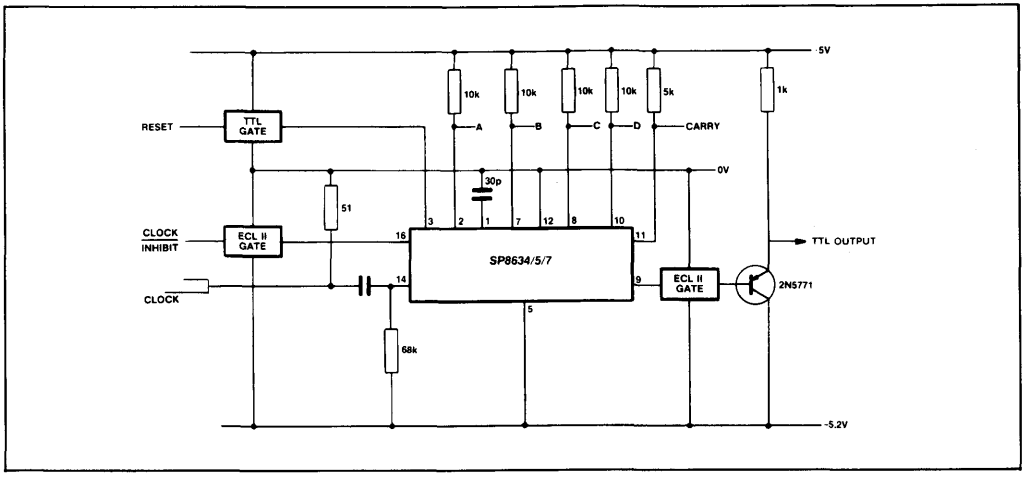


Fig.6 Typical application configuration

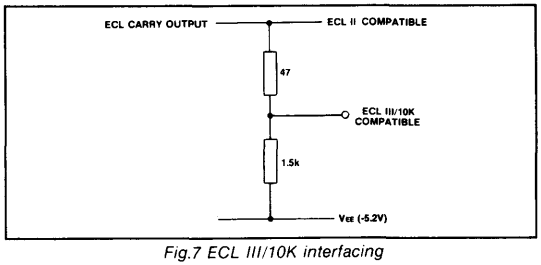


Fig.7 ECL III/10K interfacing

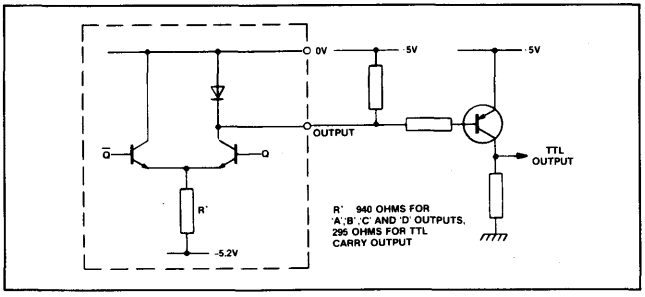


Fig.8 TTL output buffering for increased fan-out

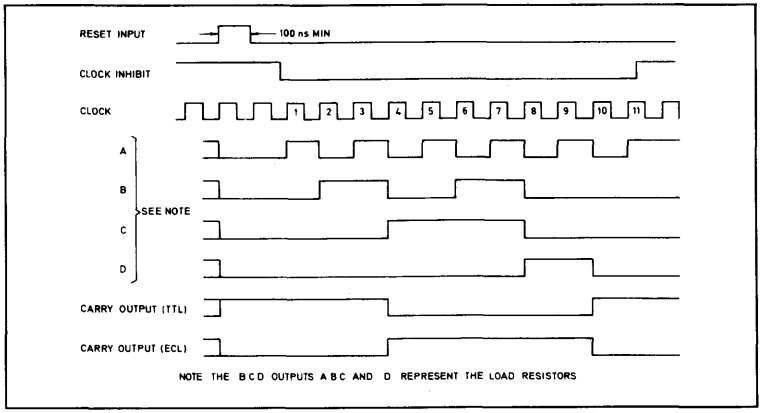


Fig.9 Timing diagram

PLESSEY
Semiconductors

SP8643A

350MHz ÷ 10/11

The SP8643 is an ECL variable modulus divider, with ECL 10K compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

The two clock inputs are interchangeable and either will act as a clock inhibit when connected to an ECL high level. Normally, one input is left open circuit and the other is AC coupled, with externally-applied bias.

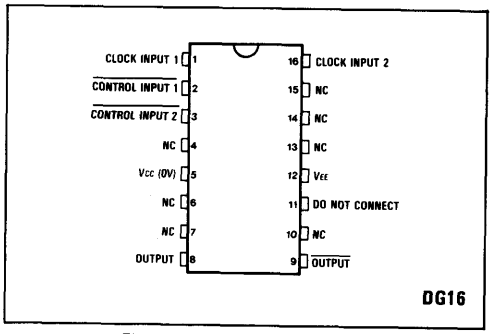


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Inputs/Outputs
- AC Coupled Input (External Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 260mW
- Temperature Range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 20mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

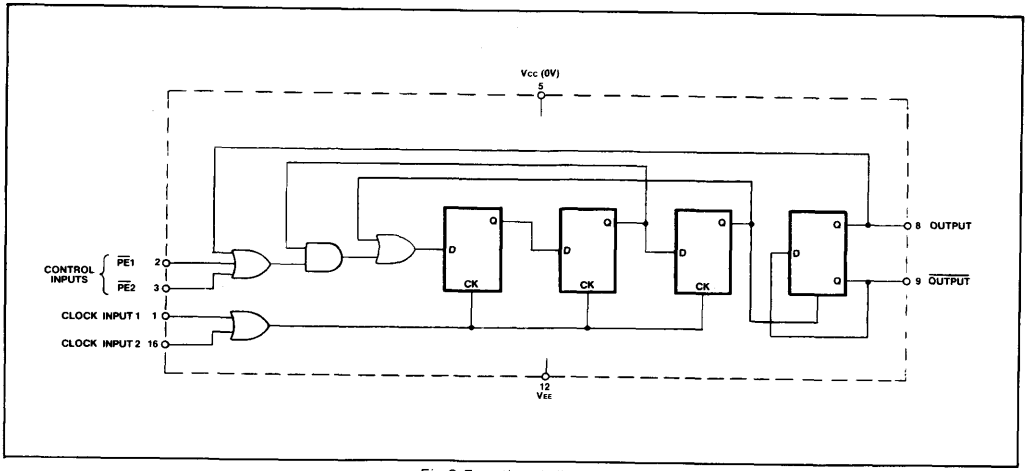


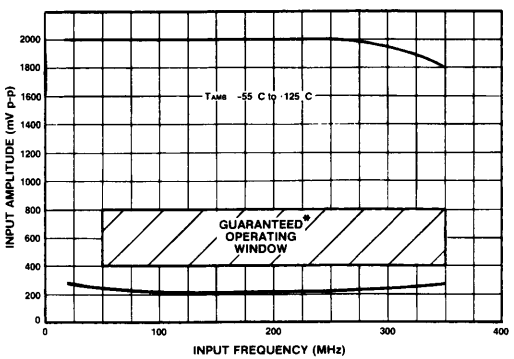
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} = -55°C to +125°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	350		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to ECL output delay	t_p		6	ns		Note 6
Set-up time	t_s	*2.5		ns		Note 6
Release time	t_r	3		ns		Note 6

NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L ⟶ H transition of control input and the next L ⟶ H clock pulse transition to ensure that +10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H ⟶ L transition of the control input and the next L ⟶ H clock pulse transition to ensure that the +11 mode is obtained.
6. Guaranteed but not tested.



* Tested as specified above.

Fig.3 Typical input characteristic of SP8643A

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

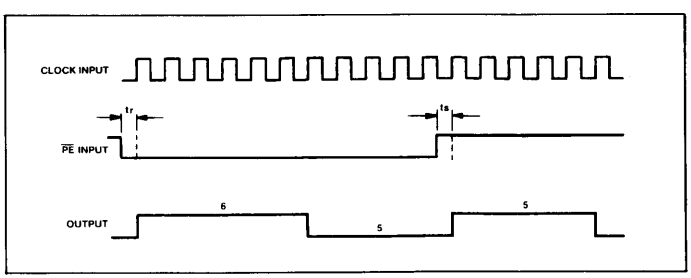


Fig.4 Timing diagram

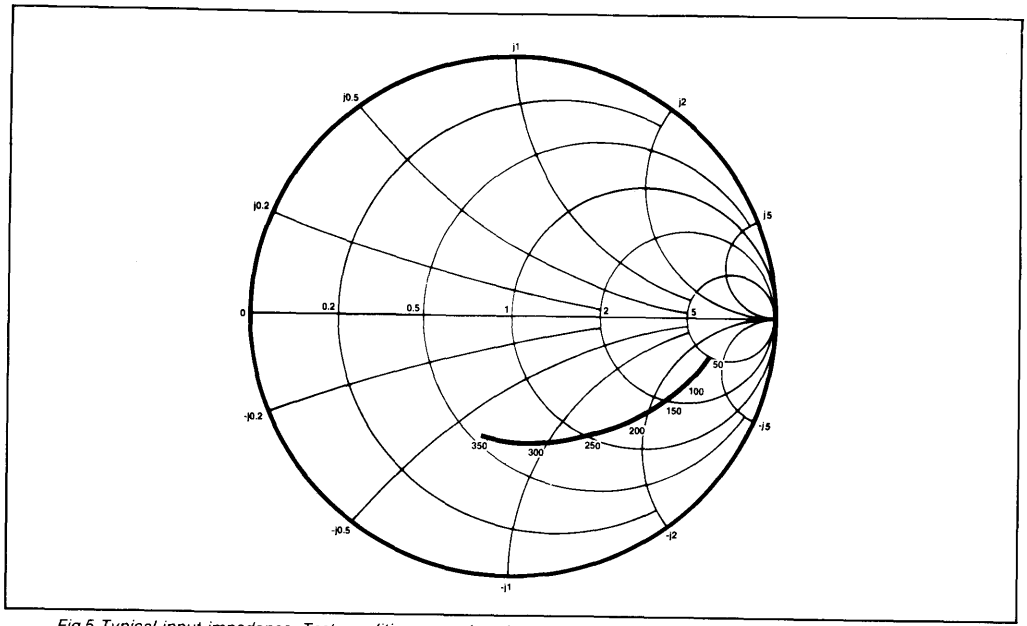


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock and control inputs are ECL III compatible. There is an internal pulldown resistor to V_{EE} of 4.3k on each input and therefore any unused input can be left open circuit when not in use but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity. If it is desirable to capacitively couple the signal source to the clock input then an external bias is required as shown in Fig. 6. The external bias voltage should be -1.3V at 25°C.
2. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. Input impedance is a function of frequency. See Fig. 5.
5. All components should be suitable for the frequency in use.

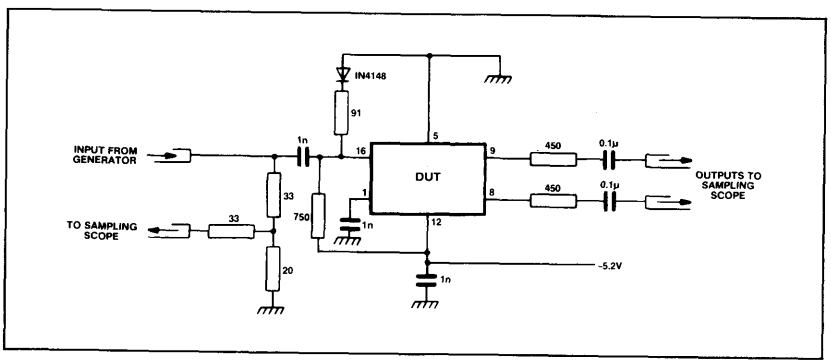


Fig.6 Test circuit

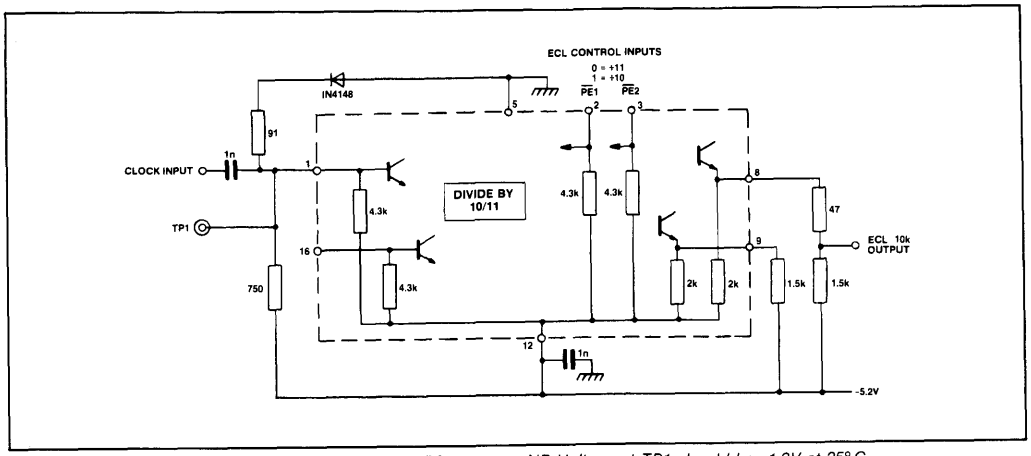


Fig.7 Typical application using ECL outputs. NB Voltage at TP1 should be -1.3V at 25° C

PLESSEY
Semiconductors

SP8647A & B

250MHz ÷ 10/11

The SP8647 is an ECL variable modulus divider, with ECL 10K and TTL/CMOS compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

The two clock inputs are interchangeable and either will act as a clock inhibit when connected to an ECL high level. Normally, one input is left open circuit and the other is AC coupled, with externally-applied bias.

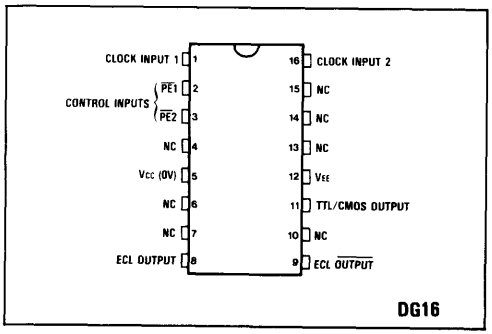


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Inputs/Outputs
- Open Collector TTL/CMOS Output
- AC Coupled Input (External Bias)

QUICK REFERENCE DATA

- Supply Voltage V_{CC}-V_{EE} : 5.2V ± 0.25V
- Power Consumption: 260mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage V_{CC} - V_{EE} : 8V
- Output Current: 20mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Open Collector Voltage (Pin 11): +12V
- Max. Clock I/P Voltage: 2.5V p-p
- Max. Open Collector Current: 15mA

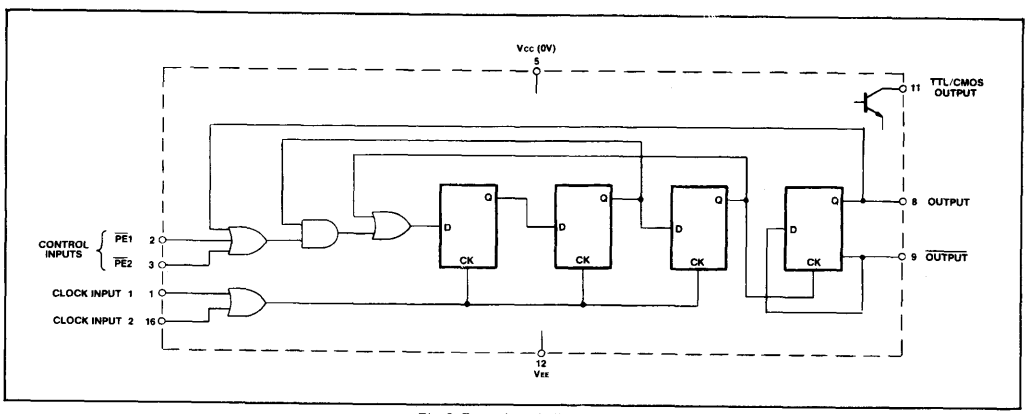


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS (ECL OPERATION)

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV p-p	Note 6
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 6
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	Note 6
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Clock and $\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
Clock and $\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to ECL output delay	t_p		6	ns		Note 7
Set-up time	t_s	2.5		ns		Note 7
Release time	t_r	3		ns		Note 7

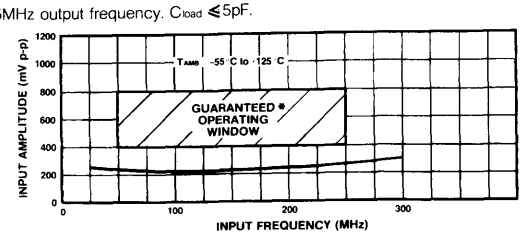
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L → H transition of control input and the next L → H clock pulse transition to ensure that ÷10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H → L transition of the control input and the next L → H clock pulse transition to ensure that the +11 mode is obtained.
6. SP8647B tested at 25°C only.
7. Guaranteed but not tested.

ELECTRICAL CHARACTERISTICS (TTL OPERATION)

Supply Voltage: V_{CC} = 5V ± 0.25V V_{EE} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	250		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		65	mA		Note 3
TTL output low voltage	V_{OL}		0.5	V	V_{CC} = +5.25V Sink current = 8mA	Note 3, 5
TTL output high voltage	V_{OH}	3.5		V	V_{CC} = +5.0V	Note 3, 5
Clock to TTL output high delay (positive going)	t_{PLH}		15	ns		Note 4
Clock to TTL output low delay (negative going)	t_{PHL}		15	ns		Note 4
Set-up time	t_s	2.5		ns		Note 4
Release time	t_r	3		ns		Note 4

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. SP8647B tested at 25°C only.
4. Guaranteed but not tested.
5. TTL output for use up to 15MHz output frequency. $C_{load} \leq 5pF$.



* Tested as specified above.

Fig.3 Typical input characteristic of SP8647A

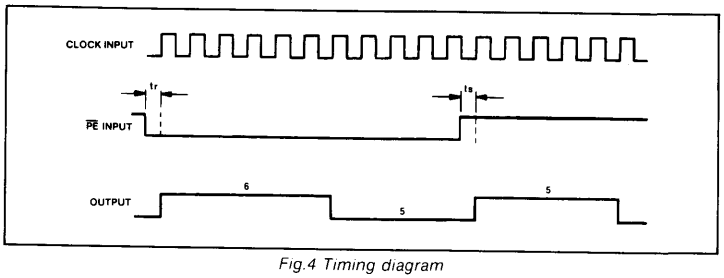


Fig.4 Timing diagram

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

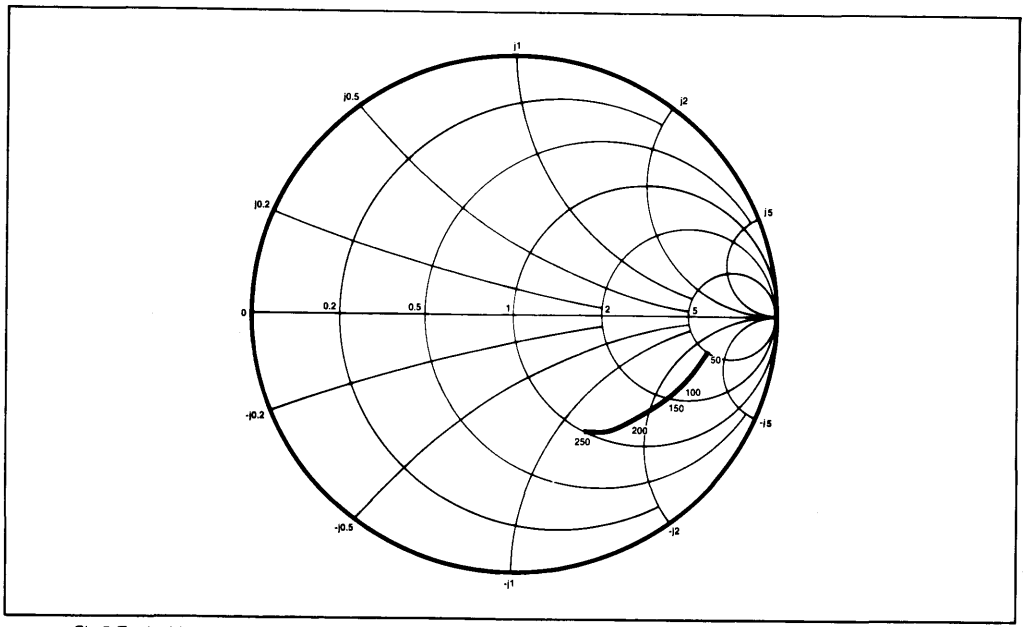


Fig.5 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock and control inputs are ECL III compatible. There is an internal pulldown resistor to V_{EE} of 4.3k on each input and therefore any unused input can be left open circuit. If it is desirable to capacitively couple the signal source to the clock then an external bias is required as shown in Fig. 6. The external bias voltage should be -1.3V at 25°C.
2. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 8.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. Input impedance is a function of frequency. See Fig. 5.
5. The TTL/CMOS O/P is a free collector, with an output rise/fall time which is a function of load resistance and load capacitance. The load capacitance should therefore be kept to a minimum and the load resistance should not be too small otherwise V_{OL} will be too great. eg TTL output current = 8mA V_{OL} = 0.5V. For CMOS outputs, the value of load resistor should be the maximum consistent with satisfactory rise times.
6. All components should be suitable for the frequency in use.

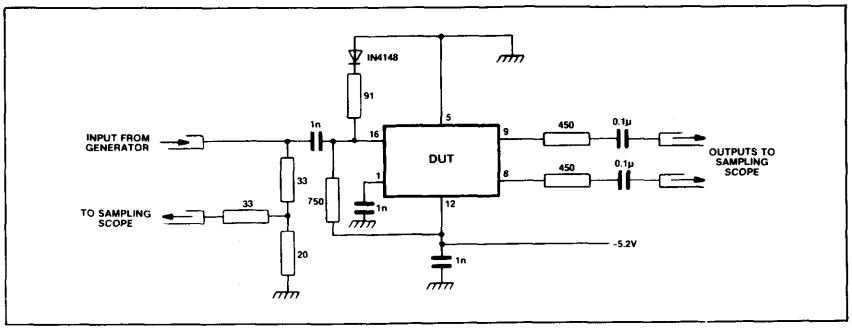


Fig.6 Test circuit

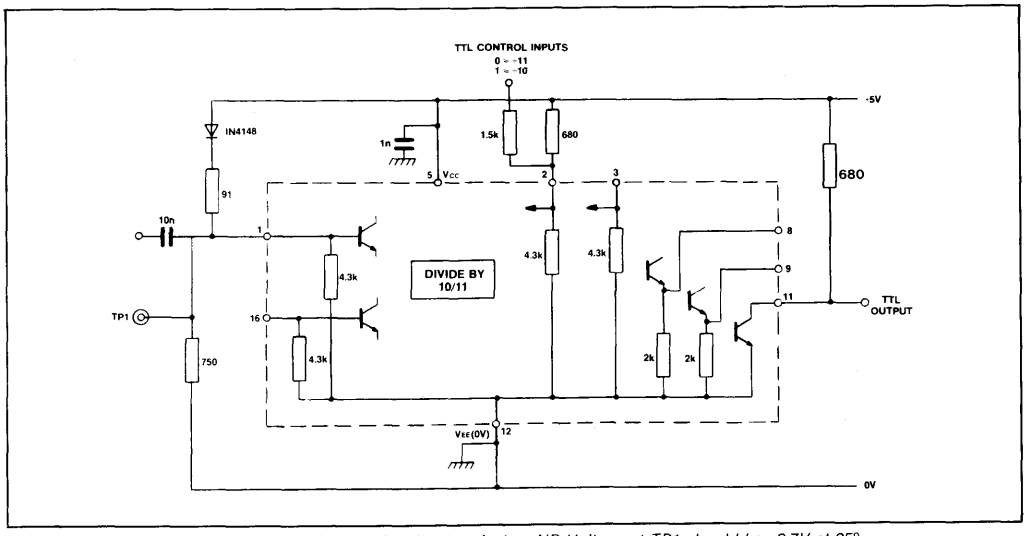


Fig.7 Typical application showing interfacing. NB Voltage at TP1 should be 3.7V at 25°

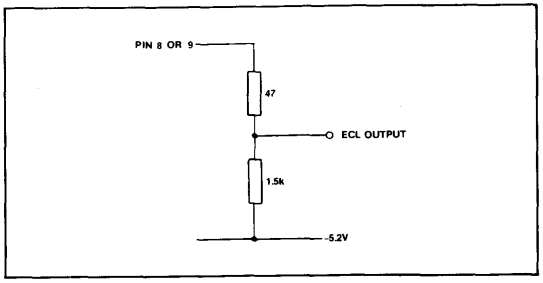


Fig.8 Interfacing to ECL 10K

PLESSEY
Semiconductors

SP8650A & B

600MHz ÷ 16

The SP8650 is an asynchronous emitter coupled logic counter which provides ECL 10K compatible outputs when external pulldown resistors are added. It requires an AC coupled input of 600mV p-p.

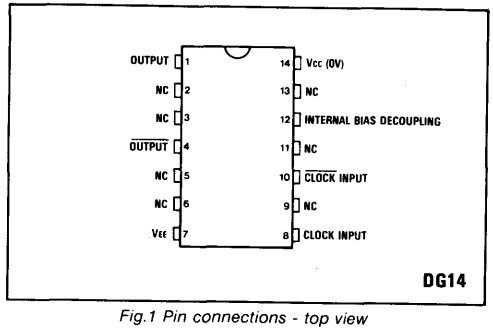


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 235mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 10mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

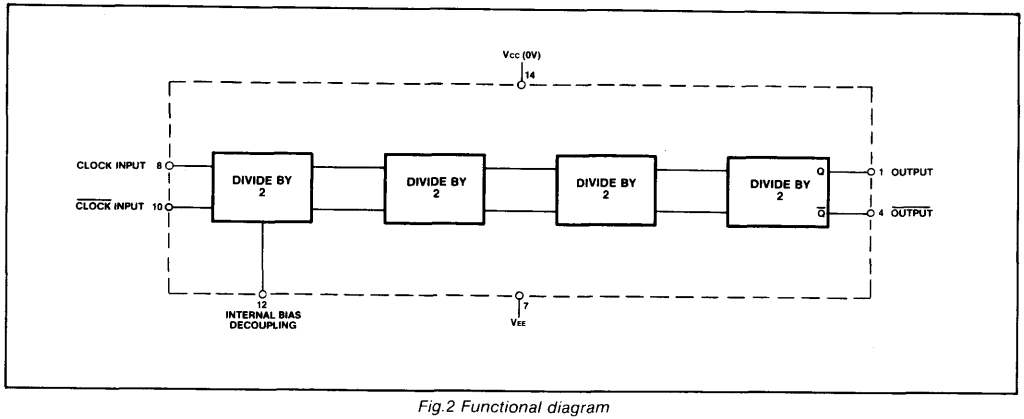


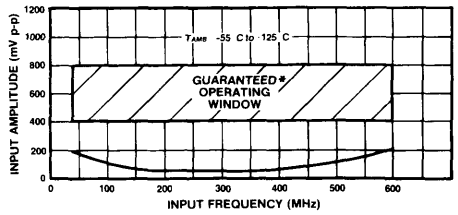
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		45	mA		Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25° only.



*Tested as specified above.

Fig.3 Typical input characteristic of SP8650A

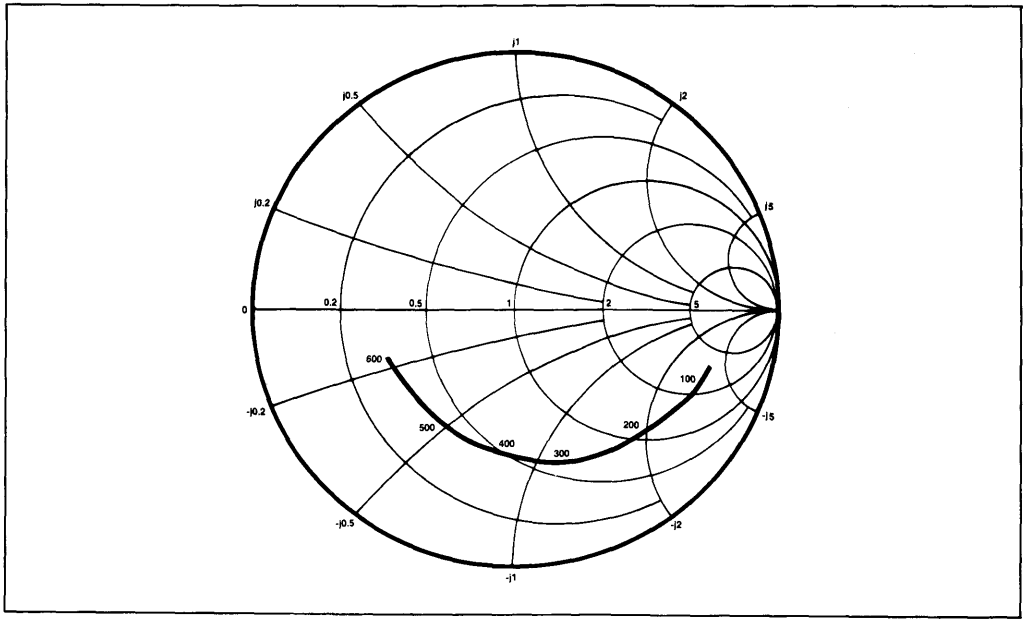


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 8 and 10) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from one of the inputs to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The outputs are compatible with ECL II. There is an internal load of 4k at each output. The output can be interfaced to ECL 10K by addition of two resistors.
5. Input impedance is a function of frequency. See Fig. 4.
6. All components should be suitable for the frequency in use.

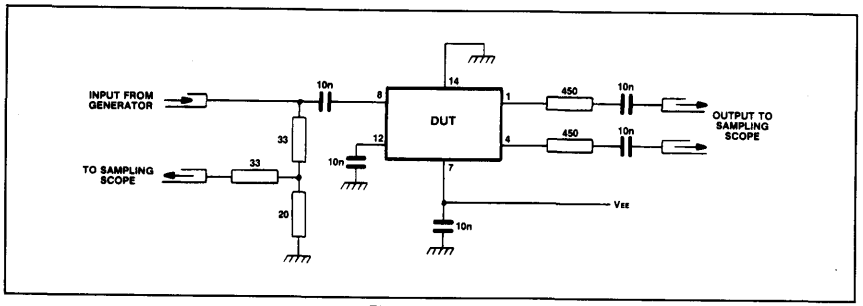


Fig.5 Test circuit

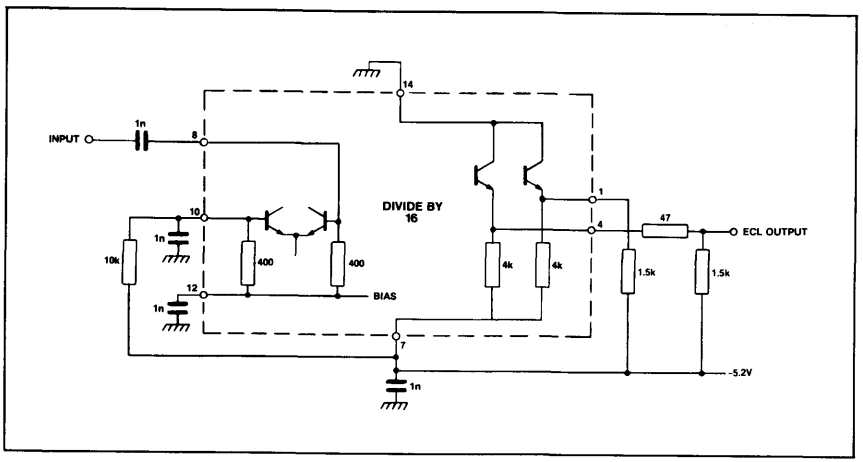


Fig.6 Typical application showing interfacing

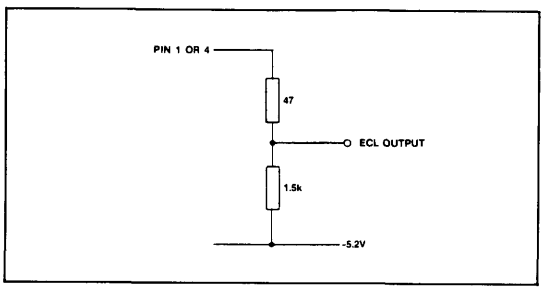


Fig.7 Interfacing to ECL 10K

PLESSEY
Semiconductors

SP8655A & B 200MHz ÷ 32
SP8657A & B 200MHz ÷ 20
SP8659A & B 200MHz ÷ 16

The SP8655, 57 and 59 are low power emitter coupled logic counters with open collector outputs capable of driving TTL or CMOS. They are available in two temperature ranges: -55°C to +125°C (A grade) and -30°C to +70°C (B grade). It has internally biased inputs.

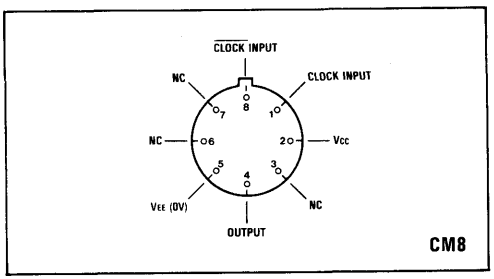


Fig.1 Pin connections - bottom view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range:
  -55°C to +125°C (A Grade)
  -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Open Collector Output Voltage: 12V
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p
- Output Sink Current: 10mA

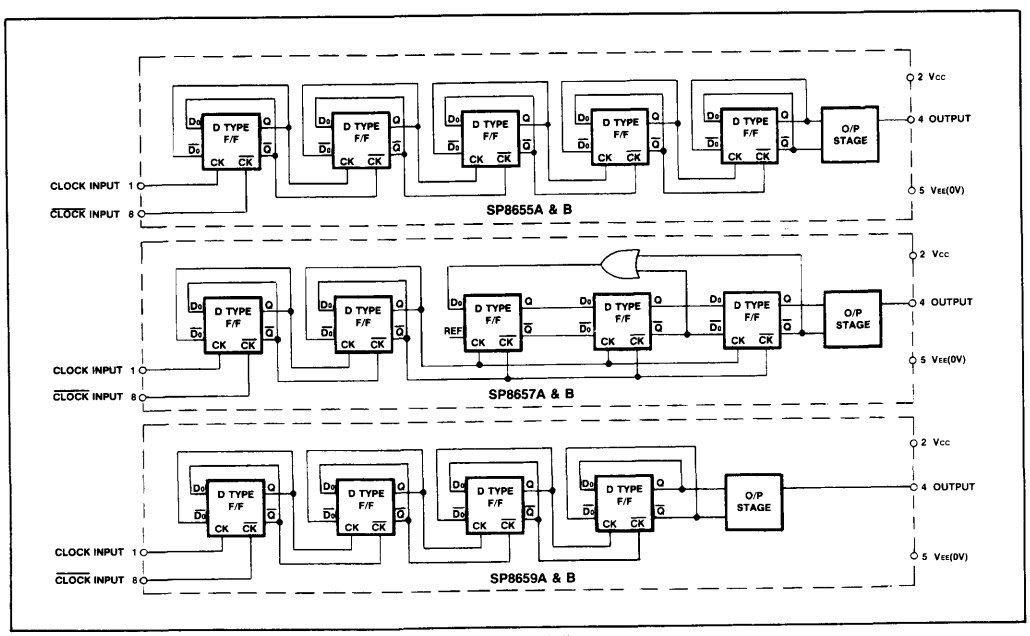


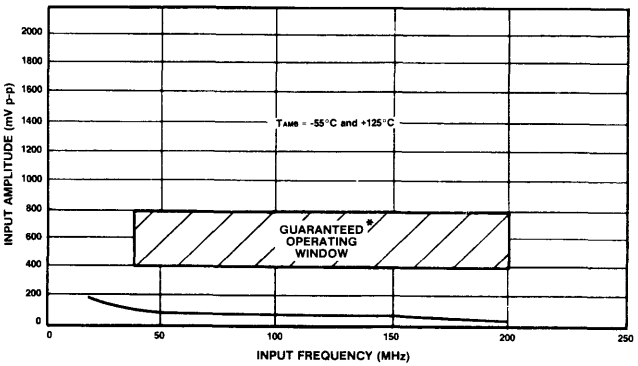
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions
		Min.	Max.		
Maximum frequency (sinewave input)	f_{max}	200		MHz	Input =400 - 800mV
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input =400 - 800mV
Power supply current	I_{EE}		13	mA	V_{CC}= 5.25V
Output high voltage	V_{OH}	7.5		V	V_{CC}= 5V Note 4 Pin 4 = 1.5kΩ to 10V
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V Pin 4 = 1.5kΩ to 10V

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).
4. Open collector output not to be used above 15MHz. $C_{load} \leq 5pF$.



*Tested as specified above.

Fig.3 Typical input characteristics

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to V_{CC} to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is typically 10ns.

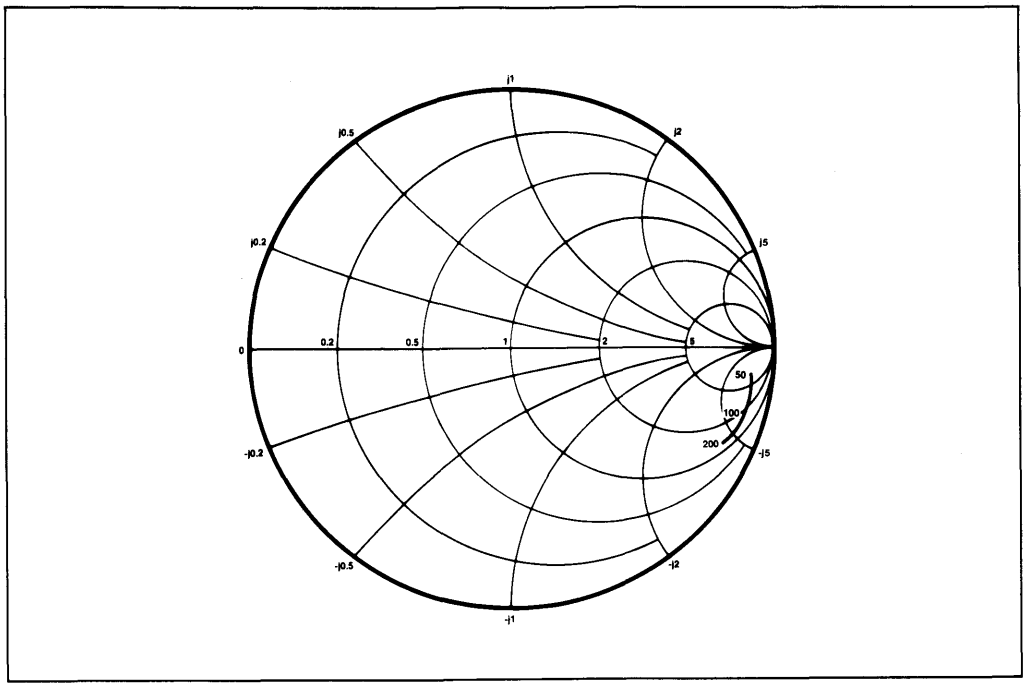


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

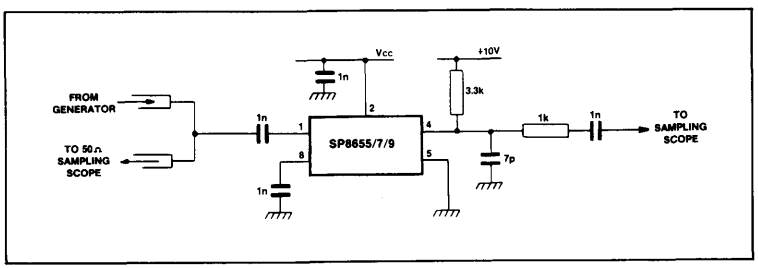


Fig.5 Test circuit

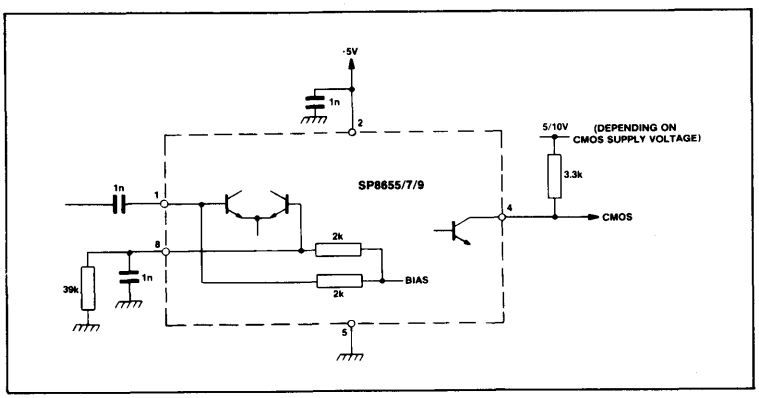


Fig.6 Typical application showing interfacing

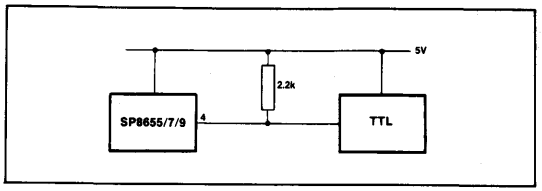


Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.

PLESSEY
Semiconductors

SP8658

200MHz ÷ 20

The SP8658 is a low power emitter coupled logic counter which provides an open collector output capable of driving TTL or CMOS. It has internally biased inputs.

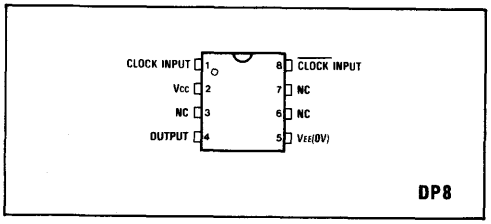


Fig.1 Pin connections - top view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output
- CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 100mW
- Temperature Range: -30°C to +70°C
- 8 Lead Plastic Package

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Open Collector Voltage: 12V
- Storage Temperature Range: -30°C to +85°C
- Max. Junction Temperature: +175°C
- Output Sink Current: 10mA
- Max. Clock I/P Voltage: 2.5V p-p

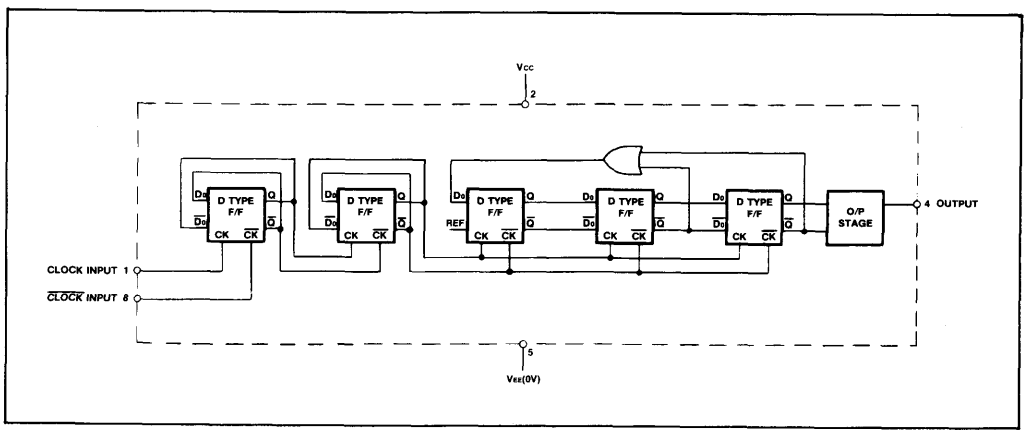


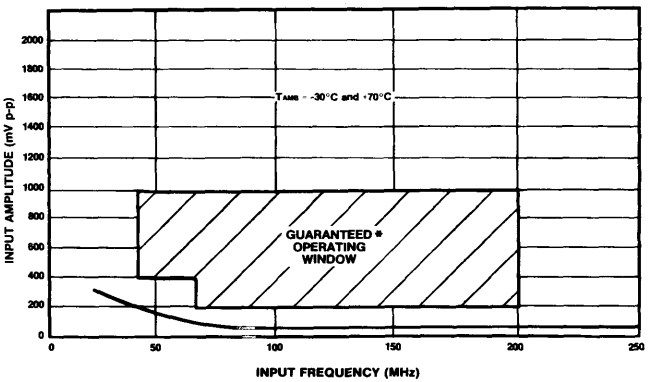
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency(sinewave I/P)	f_{max}	200		MHz	Input = 200-1000mV	
Minimum frequency(sinewave I/P)	f_{min}		40	MHz	Input = 400-1000mV	
Power supply current	I_{EE}		30	mA	V_{CC} = 5.25V	
Output high voltage	V_{OH}	7.5		V	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4

NOTES
1. Unless otherwise stated the electrical characteristics shown are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.5.
3. All characteristics above are tested at 25°C only.
4. $C_{LOAD} \leq 5pF$.



* Tested as specified above.

Fig.3 Typical input characteristics

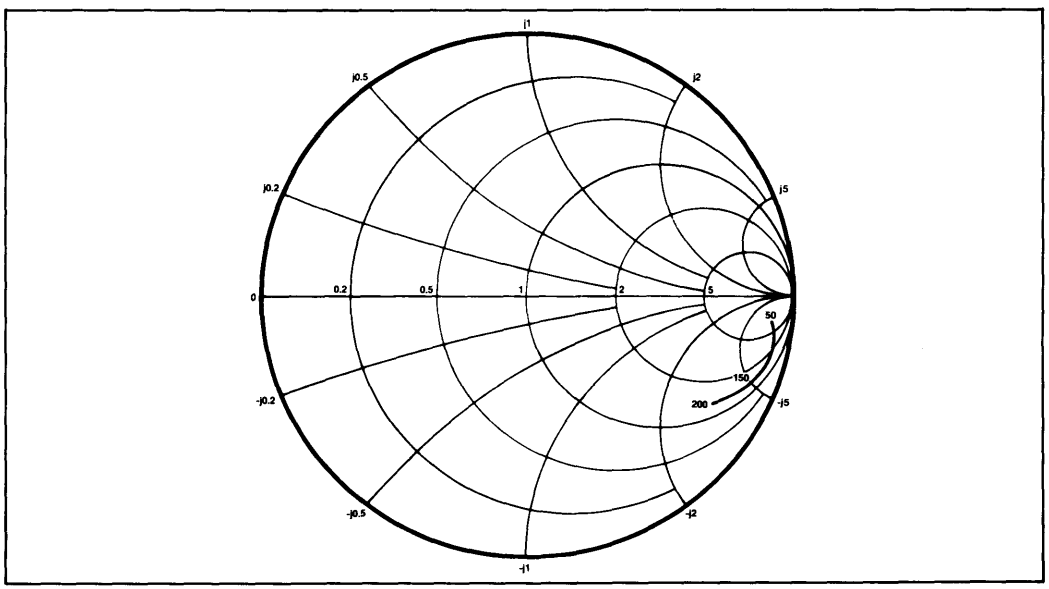


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to Vcc to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is typically 10ns.

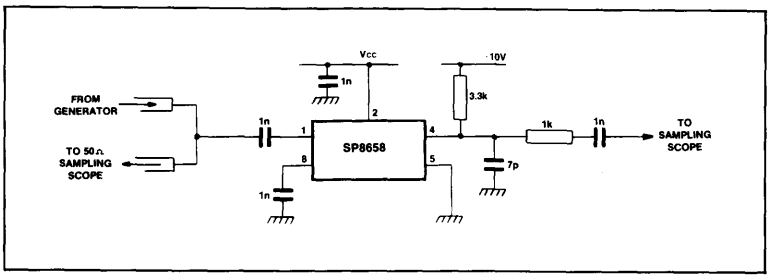


Fig.5 Test circuit

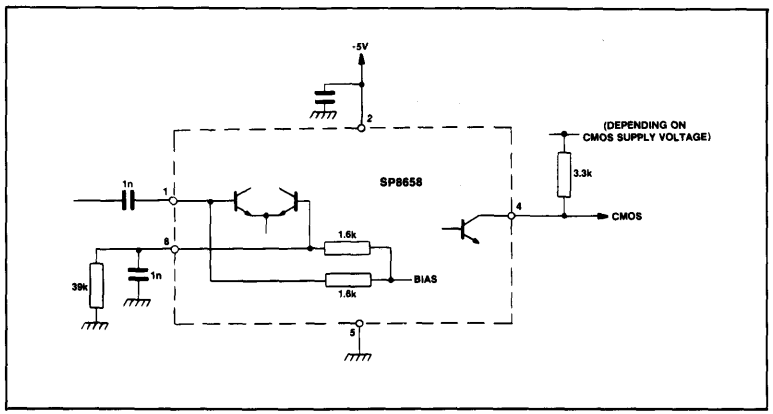


Fig.6 Typical application showing interfacing

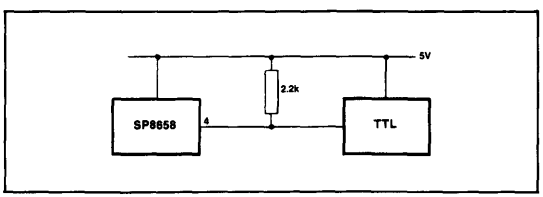


Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.

PLESSEY
Semiconductors

SP8660

150MHz ÷ 10

The SP8660 is a low power emitter coupled logic counter with an open collector output capable of driving TTL or CMOS. It has internally biased inputs and an open collector.

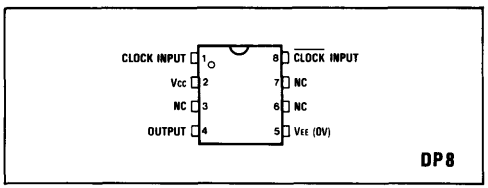


Fig.1 Pin connections - top view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range: -30°C to +70°C
- 8 Lead Plastic Package

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Open Collector Output Voltage: 12V
- Storage Temperature Range: -30°C to +70°C
- Max. Junction Temperature: +175°C
- Output Sink Current: 10mA
- Max. Clock I/P Voltage: 2.5V p-p

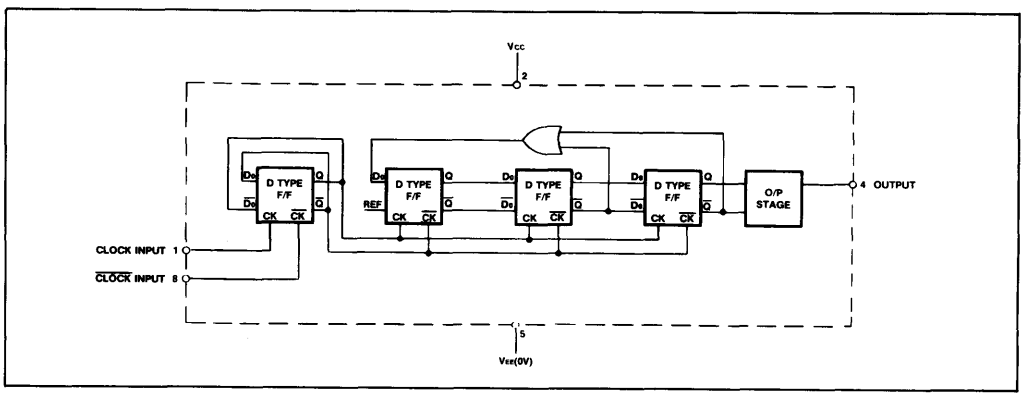


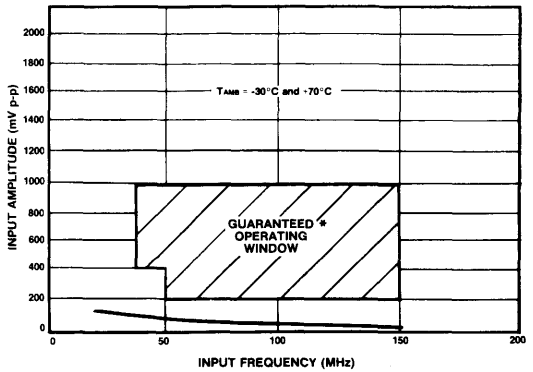
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	150		MHz	Input = 200-1000mV	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-1000mV	
Power supply current	I_{EE}		13	mA	V_{CC} = 5.25V	
Output high voltage	V_{OH}	9		V	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. All characteristics above are tested at 25°C only.
4. $C_{load} \leqslant 5pF$.



* Tested as specified above.

Fig.3 Typical input characteristics

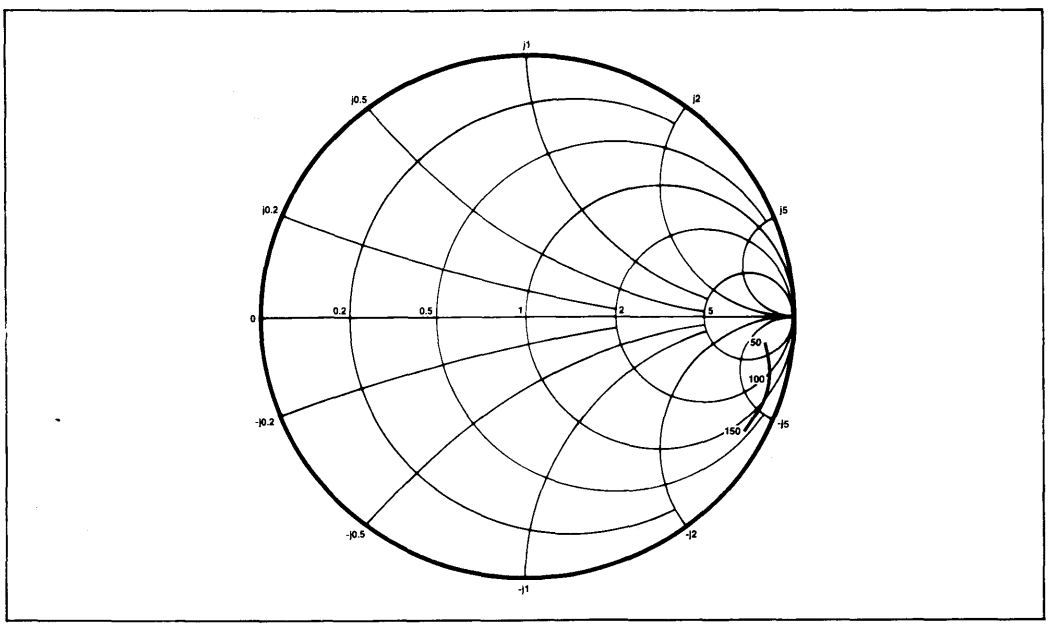


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/μs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to Vcc to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be returned to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig.4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is 10ns typically.

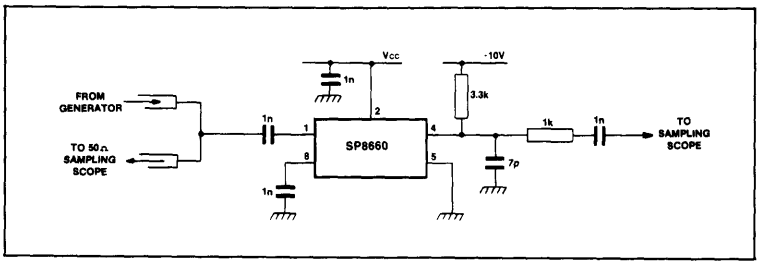


Fig.5 Test circuit

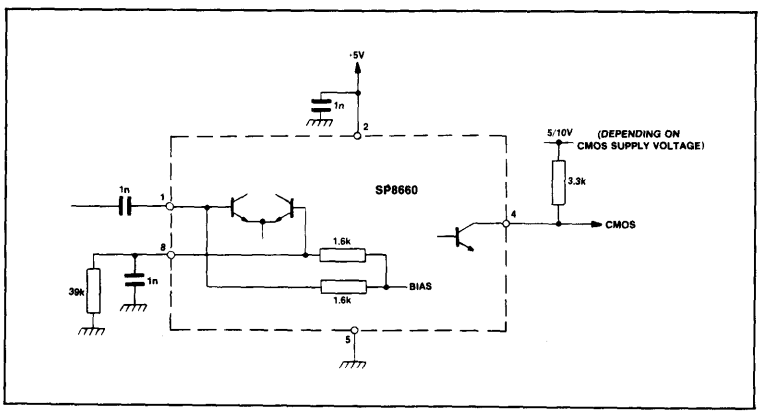


Fig.6 Typical application showing interfacing

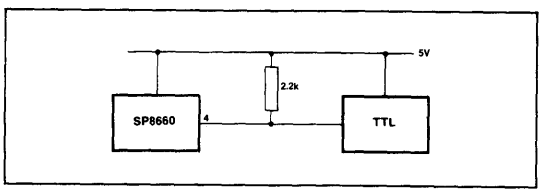


Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.

PLESSEY
Semiconductors

SP8660A & B

150MHz ÷ 10

The SP8660A/B is a low power emitter coupled logic counter with an open collector output capable of driving TTL or CMOS. The device is available in two temperature ranges: -55°C to +125°C (A grade) or -30°C to +70°C (B grade). It has internally biased inputs.

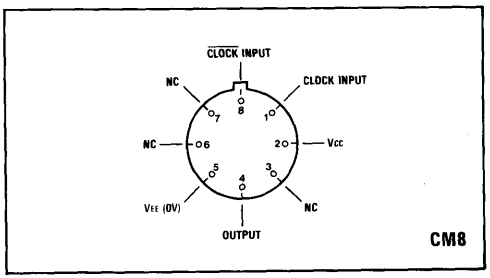


Fig.1 Pin connections - bottom view

FEATURES

- AC Coupled Inputs
- Low Power Consumption
- Open Collector Output CMOS and TTL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 50mW
- Temperature Range:
  -55°C to +125°C (SP8660A)
  -30°C to +70°C (SP8660B)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Open Collector Output Voltage: 12V
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Output Sink Current: 10mA
- Max. Clock I/P Voltage: 2.5V p-p

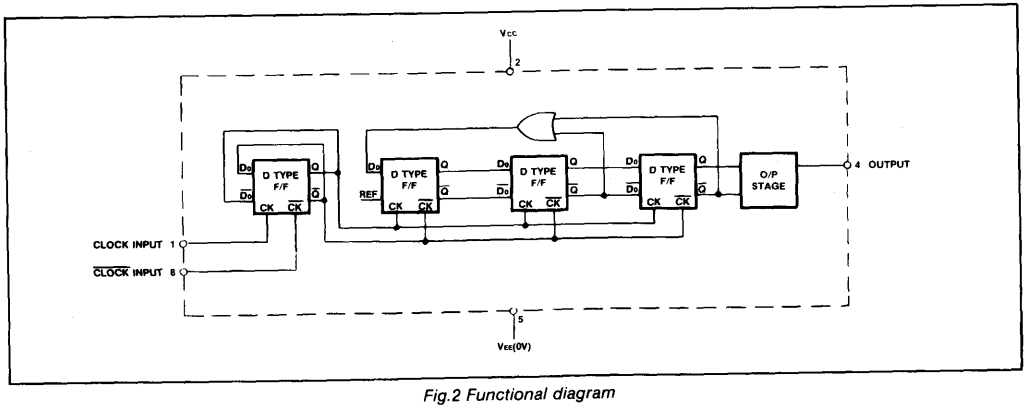


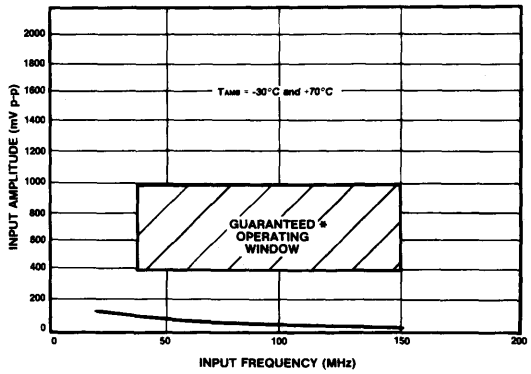
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 5.0V ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	150		MHz	Input = 400 - 800mV	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400 - 800mV	
Power supply current	I_{EE}		13	mA	V_{CC} = 5.25V	
Output high voltage	V_{OH}	7.5		V	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	Note 4
Output low voltage	V_{OL}		400	mV	V_{CC} = 5V	
					Pin 4 = 1.5kΩ to 10V	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The dynamic test circuit is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).
4. $C_{load} \leq 5pF$.



*Tested as specified above.

Fig.3 Typical input characteristic of SP8660A

OPERATING NOTES

1. The clock inputs (pin 1 and 8) should be capacitively coupled to the signal source. When driven single-ended, the input signal path is completed by connecting a capacitor from the unused input to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 39k resistor from either input to ground. If the device is driven single ended, it is recommended that the pulldown resistor be connected to the decoupled unused input. There will be a loss in sensitivity of approximately 200mV.
3. The device will operate down to DC but the input slew rate must be better than 100V/µs.
4. The open collector output will drive 3 TTL loads, and thus requires a suitable resistor to V_{CC} to maintain noise immunity. In order to ensure noise immunity on transitions, this resistor should not exceed 4.7k. For interfacing to CMOS, the open collector may be restored to a +10V line via a 3.3k resistor. The output sink current must not exceed 10mA, and the use of too low a value of resistor may lead to a loss of noise immunity, especially at low temperatures.
5. Input impedance is a function of frequency. See Fig. 4.
6. The rise time of the open collector output waveform is directly proportional to the load capacitance and load resistor value. Therefore the load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig. 5, the output rise time is approximately 20ns and fall time is 10ns typically.

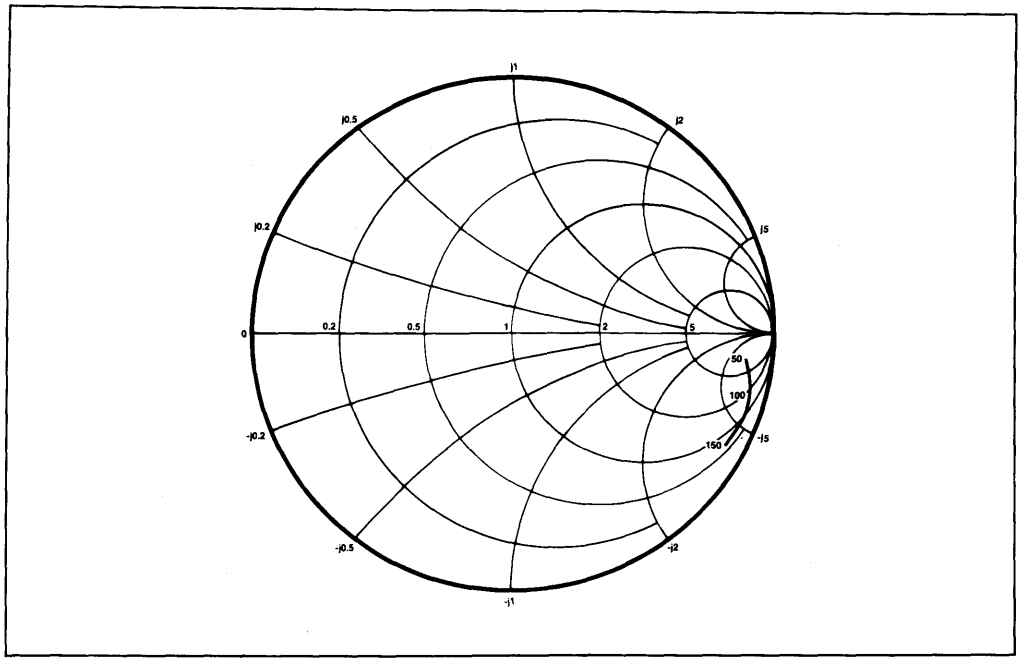


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25°C, frequencies in MHz, impedances normalised to 50 ohms.

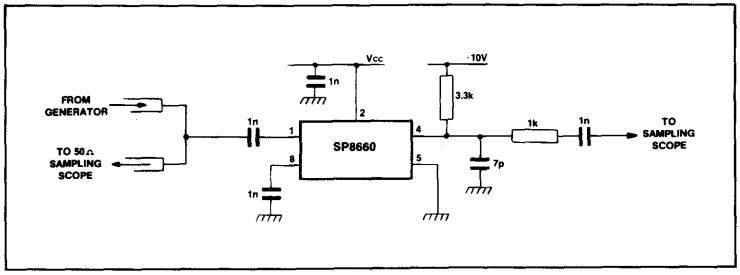


Fig.5 Test circuit

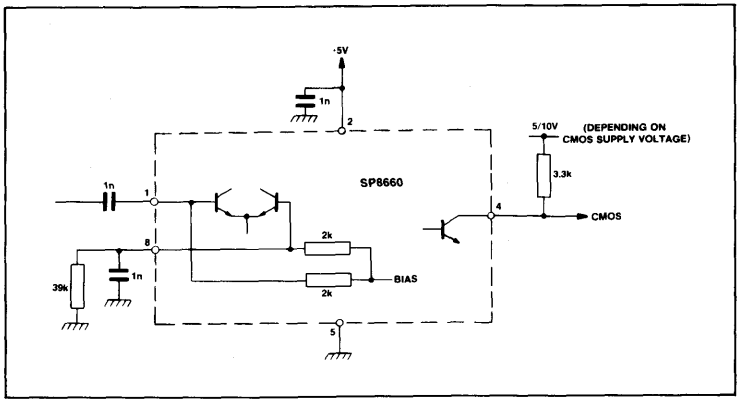


Fig.6 Typical application showing interfacing

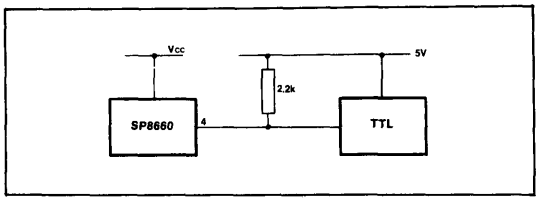


Fig.7 Interfacing to TTL. Load not to exceed 3 TTL unit loads.

PLESSEY
Semiconductors

SP8665B 1000MHz ÷ 10
SP8668B 1500MHz ÷ 10

The SP8665/8 are asynchronous ECL counters which provide ECL compatible outputs. They feature an ECL compatible input inhibit which simplifies the design of frequency counters and other instrumentation.

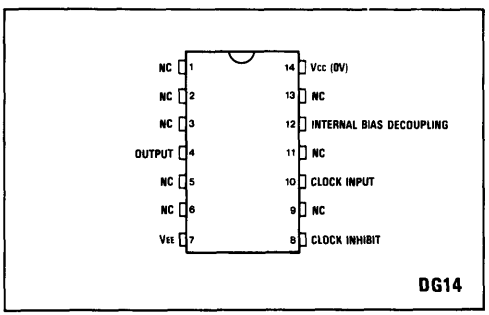


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Input
- Clock Inhibit Input

QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 500mW
- Temperature Range: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 20mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

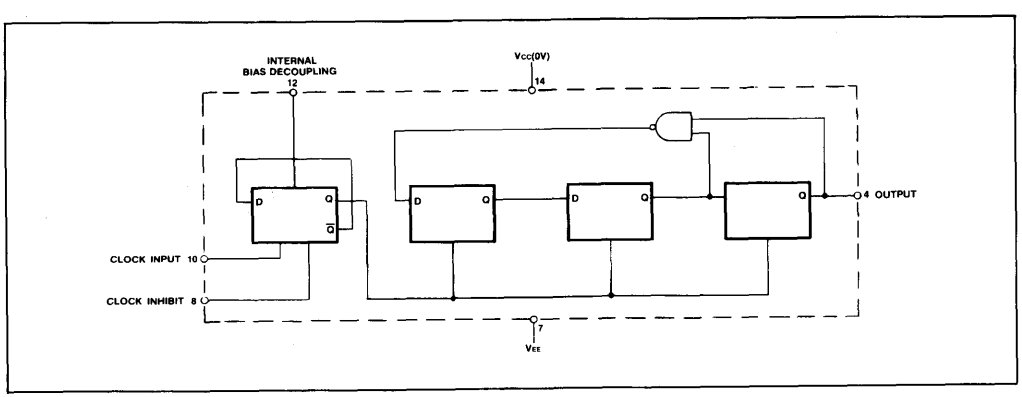


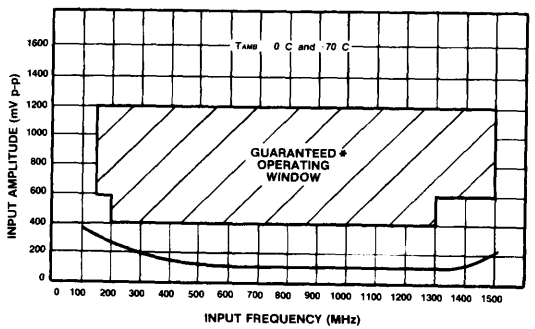
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V V_{EE} = -6.8V ± 0.3V
T_{amb} (B grade) = 0°C to +70°C

Characteristic	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Notes
Maximum frequency(sine wave I/P)	f_{max}	1.0		GHz	SP8665B	Input = 400-1200mV p-p	Note 5
		1.5		GHz	SP8668B	Input = 600-1200mV p-p	Note 5
Minimum frequency(sine wave I/P)	f_{min}		150	MHz	All	Input = 600-1200mV p-p	Note 6
Current consumption	I_{EE}		105	mA	All	V_{EE} = -6.8V	Note 6
Output low voltage	V_{OL}	-1.87	-1.5	V	All	V_{EE} = -6.8V (25°C)	
Output high voltage	V_{OH}	-0.87	-0.7	V	All	V_{EE} = -6.8V (25°C)	
Minimum output swing	V_{OUT}	500		mV	All		Note 5
Clock inhibit high threshold voltage	V_{INBH}	-0.96		V	All	V_{EE} = -6.8V (25°C)	
Clock inhibit low threshold voltage	V_{INBL}		-1.62	V	All	V_{EE} = -6.8V (25°C)	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. The temperature coefficient of V_{OH} = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
4. The temperature coefficient of V_{INB} = +0.8mV/°C but this is not tested.
5. Tested at 25°C and 70°C only.
6. Tested at 25°C only.



*Tested as specified above.

Fig.3 Typical input characteristic SP8668. The SP8665 operating window is similar except for the maximum operating frequency

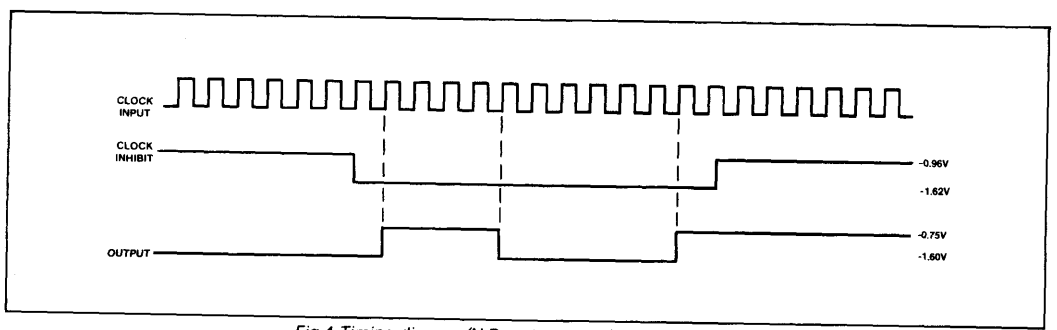


Fig.4 Timing diagram(N.B. output waveform is asymmetric)

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The clock inhibit input is compatible with standard ECL III/10K using a common 0V. A 6k pulldown resistor is included on the chip. The input should be left open to DC when not in use, but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity.
4. Input impedance is a function of frequency. See Fig. 5.
5. The emitter follower output includes an internal 3k pulldown resistor and is compatible with ECL II, but can be interfaced with ECL III/10K by the inclusion of two resistors. See Fig. 7.
6. Note that all components should be suitable for the frequency in use.
7. The circuit will operate to DC but the input slew rate must be 200V/µs or greater.

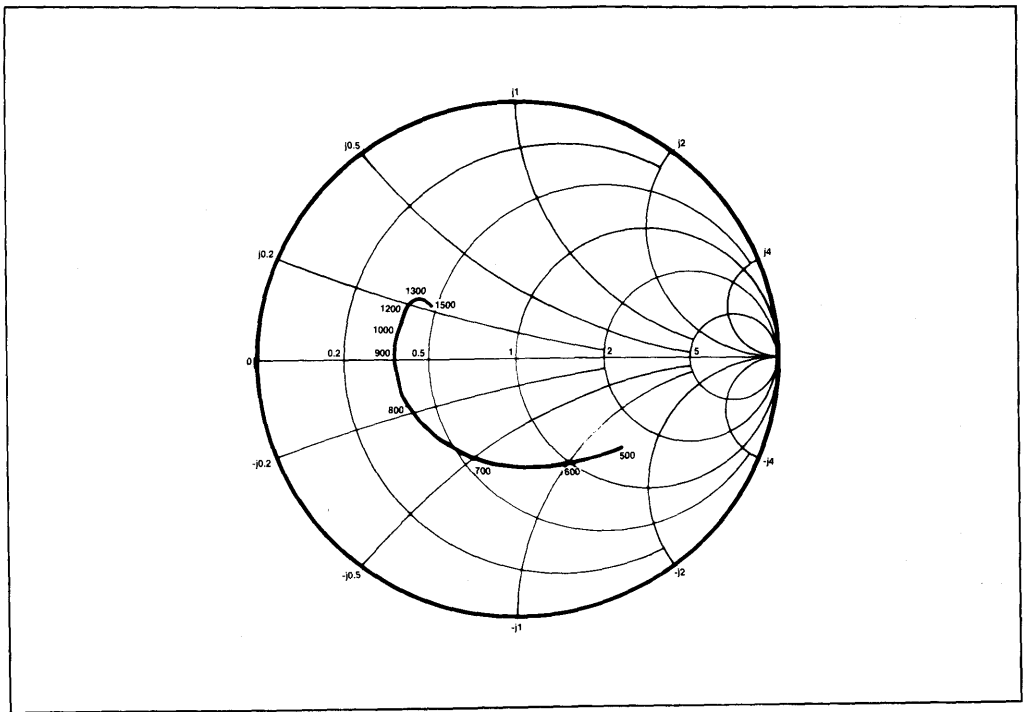


Fig.5 Typical input impedance. Test conditions: supply voltage -6.8V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

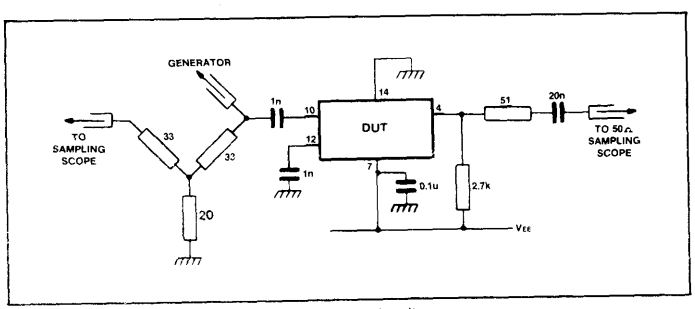


Fig.6 Test circuit

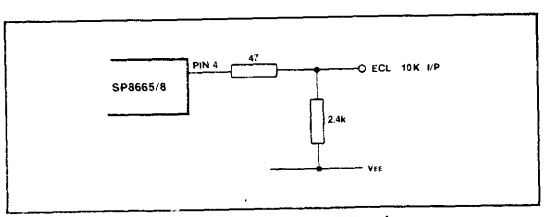


Fig.7 SP8665/8 to ECL 10K interface

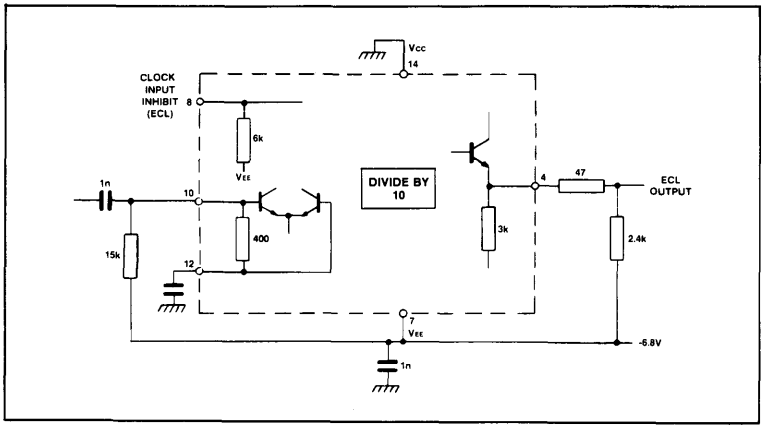


Fig.8 Typical application showing interfacing

PLESSEY
Semiconductors

SP8670A & B

600MHz ÷ 8

The SP8670 is an asynchronous emitter coupled logic counter which provides ECL 10K compatible outputs when external pulldown resistors are added. It requires an AC coupled input of 600mV p-p.

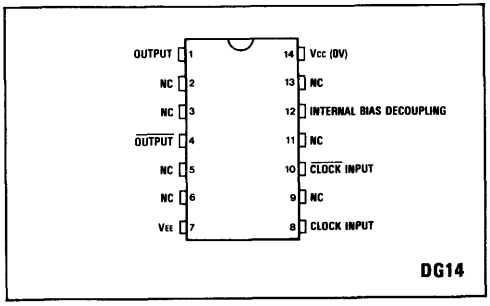


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 235mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 10mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

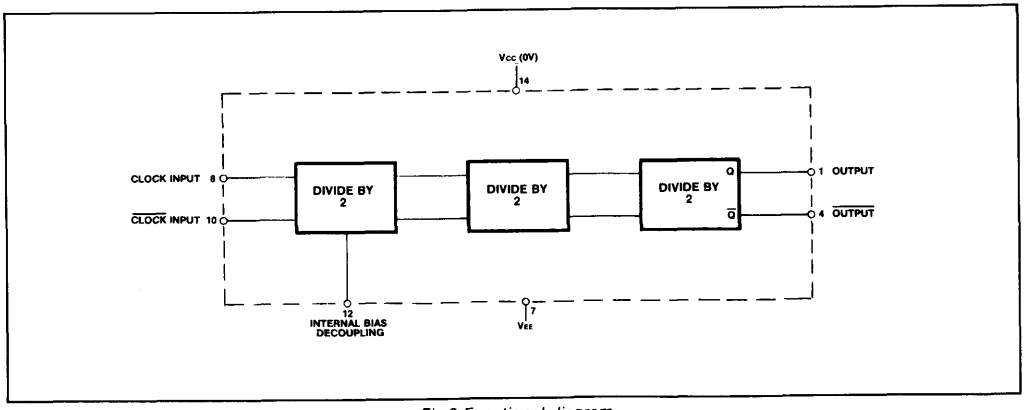


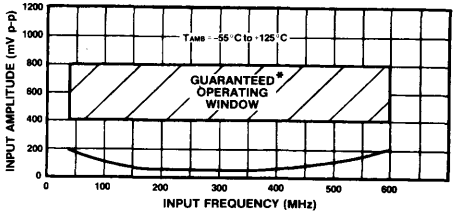
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V, V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 4
Power supply current	I_{EE}		45	mA	V_{EE} = -5.2V	Note 4
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
Minimum output swing	V_{OUT}	500		mV	V_{EE} = -5.2V	

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C and V_{OL} = +0.94mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at 25°C only.



*Tested as specified above.

Fig.3 Typical input characteristic of SP8670A

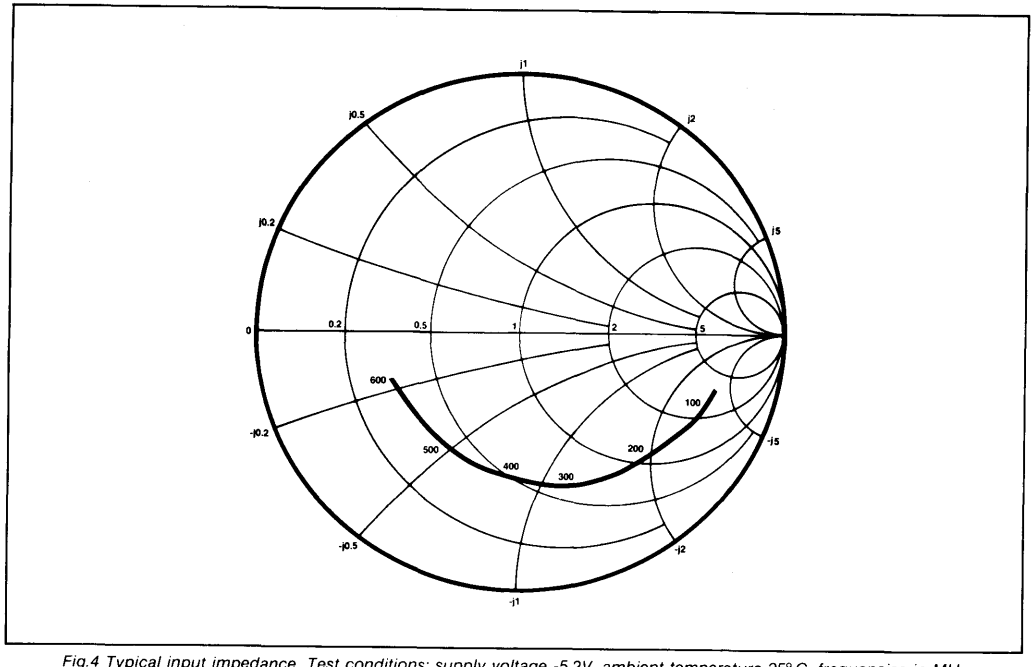


Fig.4 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs (pins 8 and 10) can be driven single-ended or differentially and should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from one of the inputs to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II. There is an internal load of 4k at each output. The output can be interfaced to ECL 10K by addition of two resistors.
5. Input impedance is shown in Fig. 4.
6. All components should be suitable for the frequency in use.

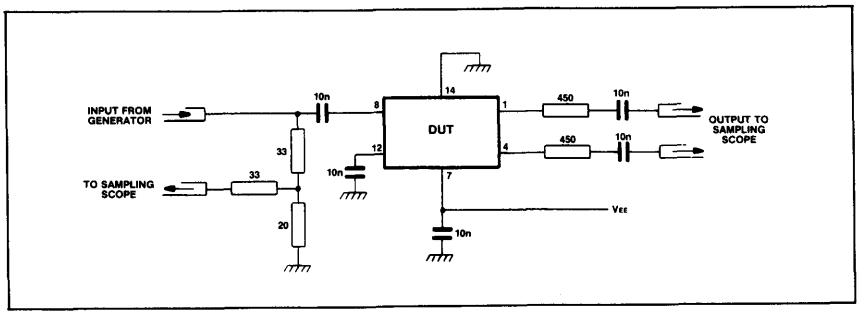


Fig.5 Test circuit

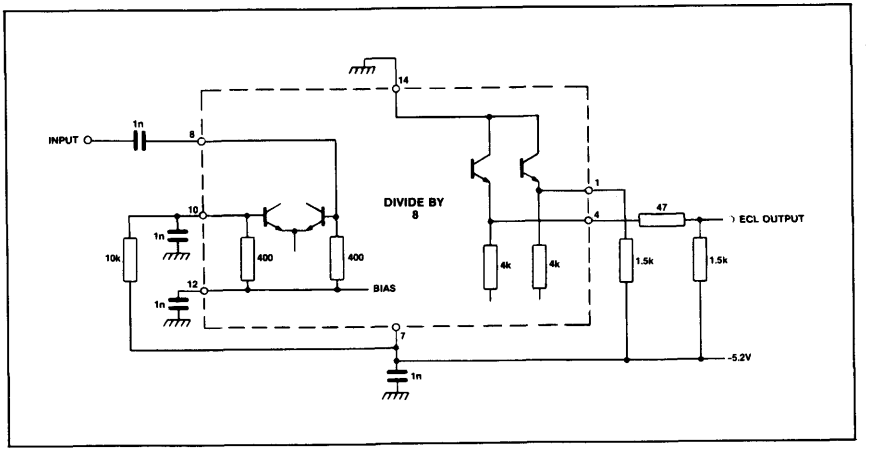


Fig.6 Typical application showing interfacing

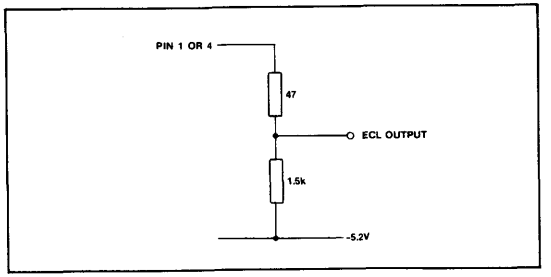


Fig.7 Interfacing to ECL 10K

PLESSEY
Semiconductors

SP8678B

1500MHz ÷ 8

The SP8678B is an asynchronous ECL counter which provides ECL compatible outputs. It features an ECL compatible input inhibit which simplifies the design of frequency counters and other instrumentation.

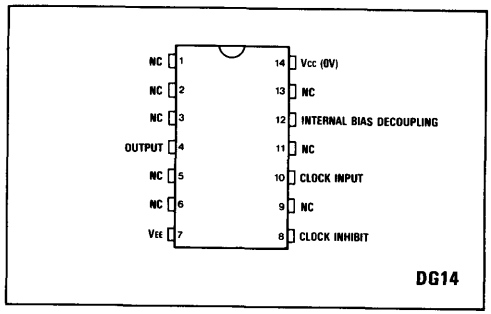


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Input
- Clock Inhibit Input

QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 475mW
- Temperature Range: 0°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 20mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

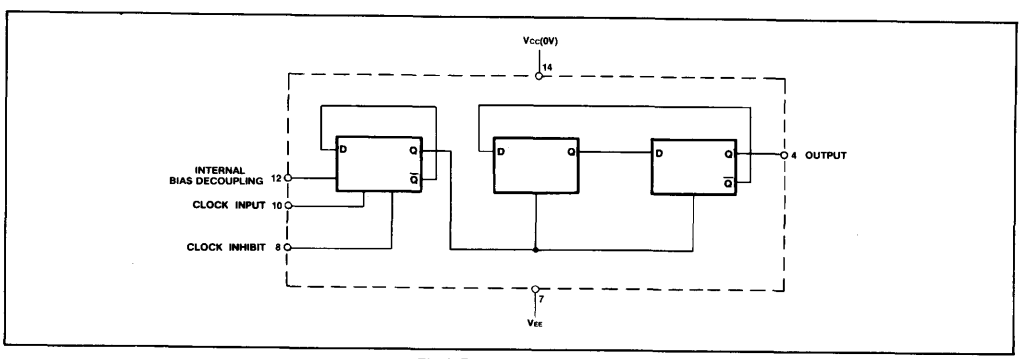


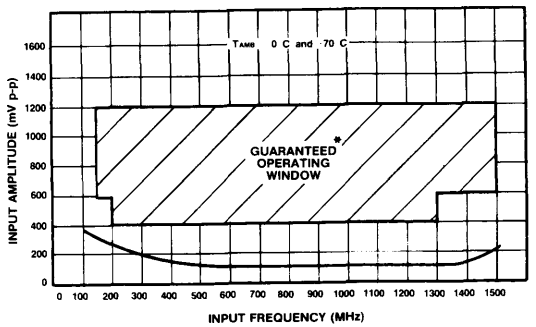
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply voltage: V_{CC} = 0V V_{EE} = -6.8V ± 0.3V
T_{amb} (B grade) = 0°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	1.5		GHz	Input =600 - 1200mV p-p	Note 5
Minimum frequency (sinewave input)	f_{min}		150	MHz	Input =600 - 1200mV p-p	Note 6
Current consumption	I_{EE}		95	mA	V_{EE} = -6.8V	Note 6
Output low voltage	V_{OL}	-1.87	-1.5	V	V_{EE} = -6.8V(25° C)	
Output high voltage	V_{OH}	-0.87	-0.7	V	V_{EE} = -6.8V(25° C)	
Minimum output swing	V_{OUT}	500		mV		Note 5
Clock inhibit high threshold voltage	V_{INBH}	-0.96		V	V_{EE} = -6.8V(25° C)	
Clock inhibit low threshold voltage	V_{INBL}		-1.62	V	V_{EE} = -6.8V(25° C)	

NOTES
1. Unless otherwise stated, the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig. 6.
3. The temperature coefficient of V_{OH} = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
4. The temperature coefficient of V_{INB} = +0.8mV/°C but this is not tested.
5. Tested at 25°C and 70°C only.
6. Tested at 25°C only.



*Tested as specified above.

Fig.3 Typical input characteristics

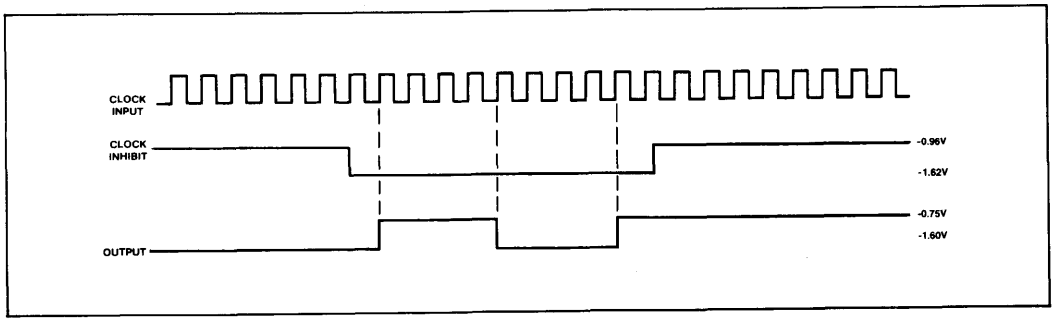


Fig.4 Timing diagram

OPERATING NOTES

1. The clock input (pin 10) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 12, to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 10 to Pin 7). This will reduce the input sensitivity by approximately 100mV.
3. The clock inhibit input is compatible with standard ECL III/10K using a common 0V. A 6k pulldown resistor is included on the chip. The input should be left open to DC when not in use, but should be bypassed for RF signals with a 1nF capacitor to ensure maximum noise immunity.
4. Input impedance is a function of frequency. See Fig. 5.
5. The emitter follower output includes an internal 3k pulldown resistor and is compatible with ECL II, but can be interfaced with ECL III/10K by the inclusion of two resistors. See Fig. 7.
6. Note that all components should be suitable for the frequency in use.
7. The circuit will operate to DC but the input slew rate must be 200V/µs or greater.

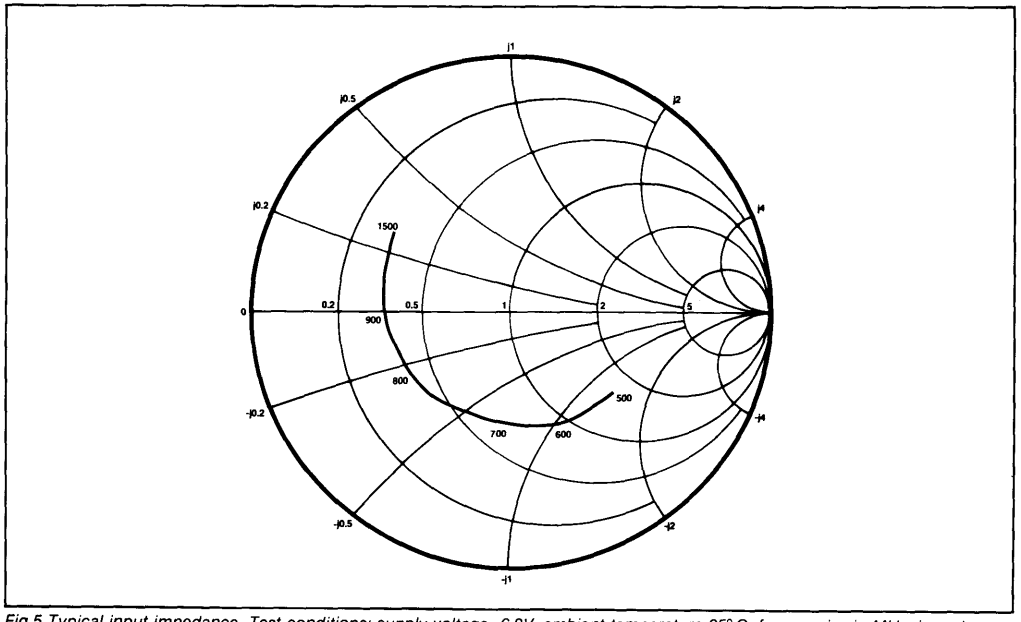


Fig.5 Typical input impedance. Test conditions: supply voltage -6.8V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

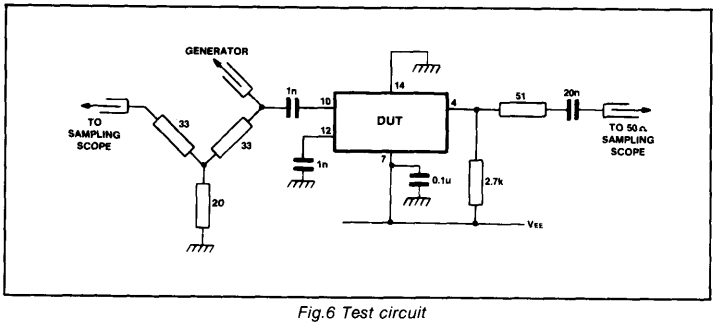


Fig.6 Test circuit

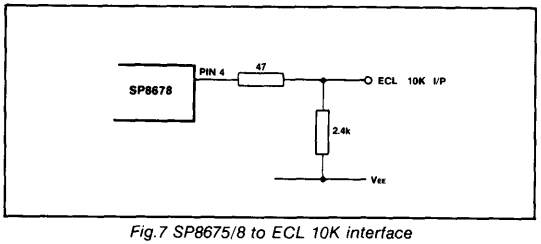


Fig.7 SP8675/8 to ECL 10K interface

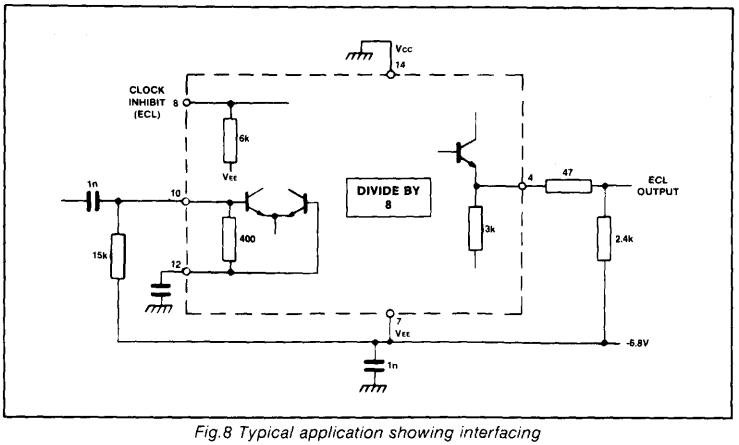


Fig.8 Typical application showing interfacing

PLESSEY
Semiconductors

SP8680A&B

600MHz ÷ 10/11

The SP8680 is an ECL counter with both ECL 10K and TTL compatible outputs. The circuit can operate from either ECL or TTL supplies. The division ratio is controlled by two control inputs (PE1 and PE2) which are ECL compatible. The counter will divide by 10 when either control input is in the high state and by 11 when both inputs are low. The counter can also be set to the eleventh state by applying a high level to the master set input.

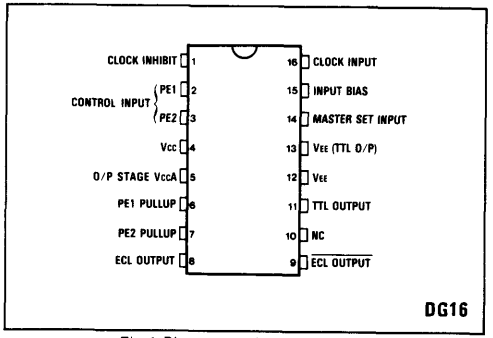


Fig.1 Pin connections - top view

FEATURES

- Very High Speed - 650MHz Typ.
- ECL and TTL Compatible Outputs
- DC or AC Clocking
- Clock Enable
- Divide By 10 or 11
- Asynchronous master set
- Equivalent to Fairchild 11C90

QUICK REFERENCE DATA

- Supply Voltage: 5V +0.5V -0.25V
  or -5V -0.5V +0.25V
- Power Consumption: 420mW
- Temperature: -55°C to +125°C (A Grade)
  0°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- ECL Output Source Current: 50mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- TTL Output Sink Current: 30mA
- Max. Clock I/P Voltage: 2.5V p-p

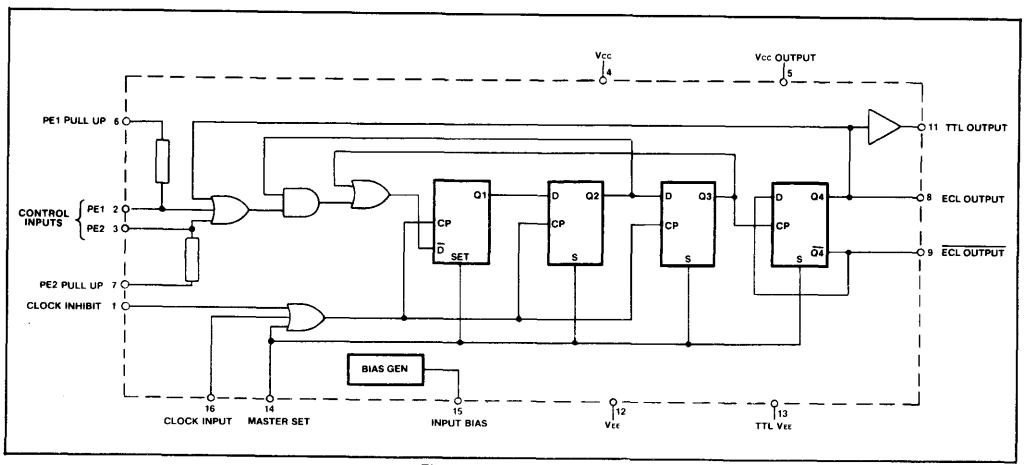


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS
TTL OPERATION

Supply Voltage: V_{CC} = $V_{CC}A$ = 4.75 to 5.5V V_{EE} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Notes
Maximum frequency sinewave input	f_{max}		550	MHz	SP8680A	Clock input AC coupled = 350mVp-p	Note 4
			575	MHz	SP8680B		Note 4
Minimum frequency sinewave input	f_{min}	10		MHz	Both	Clock input AC coupled = 600mVp-p	Note 5
Power supply current	I_{EE}		105	mA	Both	V_{CC} = V_{CC} max. Pins 6,7,13 open circuit	Note 4
Power supply current including TTL stage	I_{EE}		111	mA	Both	V_{CC} = V_{CC} max. Pins 6,7 open circuit	Note 4
TTL output high voltage	V_{OH}	2.3		V	Both	V_{CC} = V_{CC} min. I_{OH} = -640µA	Note 4
TTL output low voltage	V_{OL}		0.5	V	Both	V_{CC} = V_{CC} max. I_{OL} = 20mA	Note 4
Input high voltage PE1 and PE2 inputs	V_{INH}	3.9		V	Both	V_{CC} = 5.0V (25°C)	
Input low voltage PE1 and PE2 inputs	V_{INL}		3.5	V	Both	V_{CC} = 5.0V (25°C)	
Input low current PE1 and PE2 inputs	I_{IL}	-4		mA	Both	V_{CC} = V_{CC} max(25°C) Pins 6,7 = V_{CC} V_{IN} = 0.4V	
Propagation delay CP to Q TTL	t_{pHL} t_{pLH}	6	14	ns	Both	V_{CC} = 5.0V (25°C)	Note 5
Propagation delay MS to Q TTL	t_p		17	ns	Both	V_{CC} = 5.0V (25°C)	Note 5
Mode control set-up time	t_s	4		ns	Both	V_{CC} = 5.0V (25°C)	Note 5
Mode control release time	t_r	4		ns	Both	V_{CC} = 5.0V (25°C)	Note 5
TTL output rise time(20%-80%)	t_{TLH}		5	ns	Both	V_{CC} = 5.0V (25°C)	Note 5
TTL output fall time(80%-20%)	t_{THL}		5	ns	Both	V_{CC} = 5.0V (25°C)	Note 5

ELECTRICAL CHARACTERISTICS
ECL OPERATION

Supply Voltage: V_{EE} = -4.75V to -5.5V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Notes
Maximum frequency sinewave input	f_{max}		550	MHz	SP8680A	Clock input AC coupled = 350mVp-p	Note 4
			575	MHz	SP8680B		Note 4
Minimum frequency sinewave input	f_{min}	10		MHz	Both	Clock input AC coupled = 600mVp-p	Note 5
Power supply current	I_{EE}		105	mA	Both	V_{CC} = V_{CC} max. Pins 6,7,13 open circuit	Note 4
ECL output high voltage	V_{OH}	-0.93	-0.78	V	Both	V_{EE} = -5.2V (25°C) Load = 100Ω to -2V	
ECL output low voltage	V_{OL}	-1.85	-1.62	V	Both	V_{EE} = -5.2V (25°C) Load = 100Ω to -2V	
Input high voltage	V_{INH}	-1.095	-0.81	V	Both	V_{EE} = -5.2V (25°C)	
Input low voltage	V_{INL}	-1.85	-1.475	V	Both	V_{EE} = -5.2V (25°C)	

ELECTRICAL CHARACTERISTICS (CONT)
ECL OPERATION

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Input low currents	I_{IL}	0.5		μA	25° C	
Input high current						
Clock and MS	I_H		400	μA	V_{IN} = -1.85V(25° C)	
PE1 and PE2	I_H		250	μA	V_{IN} = -0.8V(25° C)	
Propagation delay CP to Q4	t_{pLH}		3	ns	Load = 100Ω to -2V(25° C)	Note 5
Propagation delay MS to Q4	t_{pLH}		6	ns	25° C	Note 5
Mode control set-up time	t_s	4		ns	25° C	Note 5
Mode control release time	t_r	4		ns	25° C	Note 5
ECL output rise time (20 % - 80 %)	t_{TLH}		2	ns	25° C	Note 5
ECL output fall time (80 % - 20 %)	t_{THL}		2	ns	25° C	Note 5

NOTES
1. Unless otherwise stated, the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.2mV/°C, V_{OL} = +0.24mV/°C and of V_{IN} = +0.8mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. Tested at 25°C and +125°C only (+70°C for B grade).
5. Guaranteed but not tested.

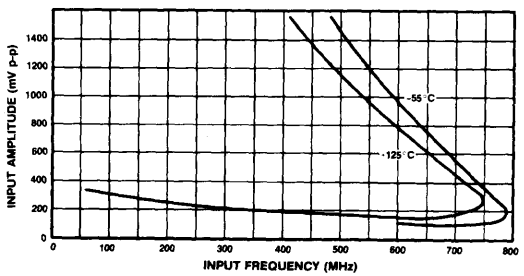
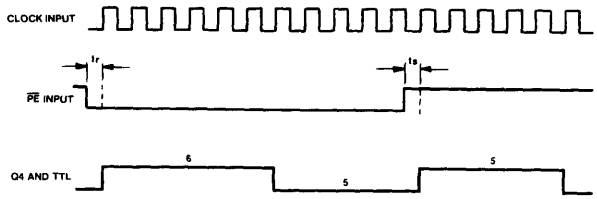


Fig.3 Typical input sensitivity SP8680A



MS	CLOCK INH.	PE1	PE2	OUTPUT RESPONSE
H	X	X	X	ALL OUTPUTS SET HIGH
L	H	X	X	HOLD
L	L	L	L	÷11
L	L	H	L	÷10
L	L	L	H	÷10
L	L	H	H	÷10

X = DON'T CARE

Fig.4 Truth table and timing diagram SP8680

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.

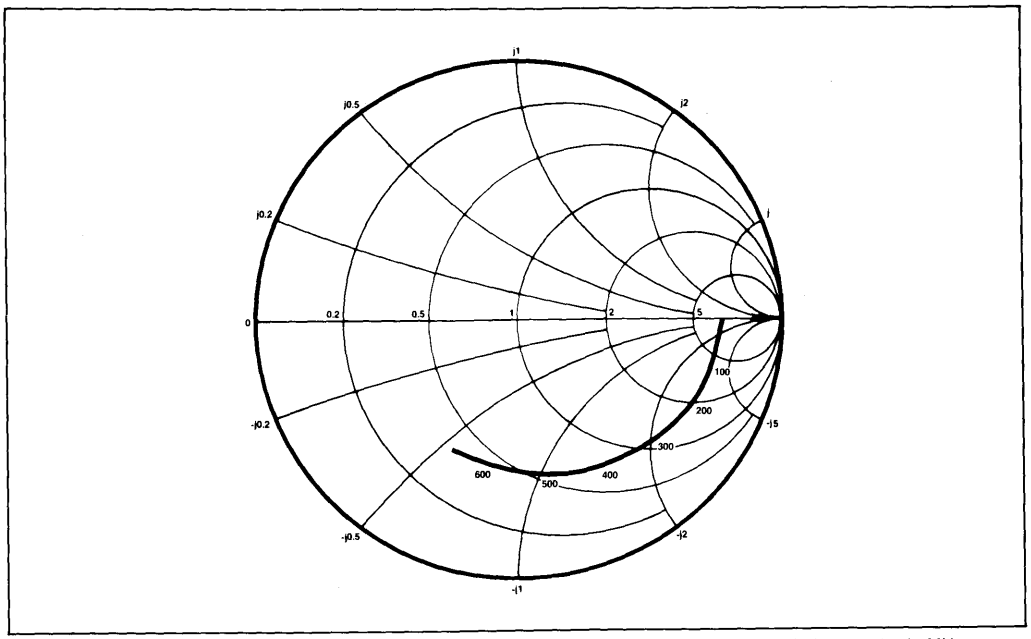


Fig.5 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

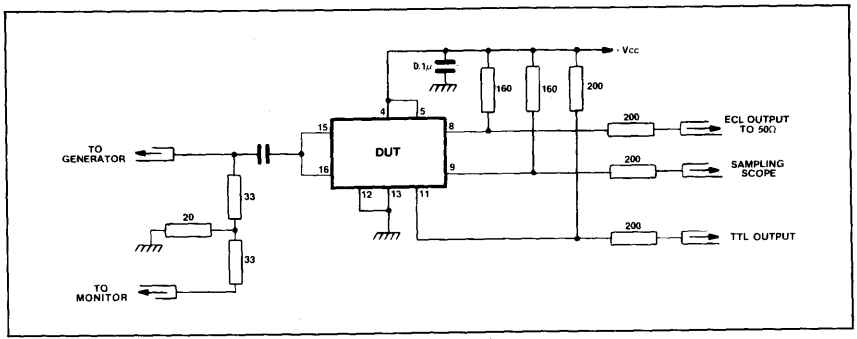


Fig.6 Test circuit

OPERATING NOTES

1. The clock input, which is ECL 10K compatible throughout the temperature range, can also be directly coupled to TTL as shown in Fig. 9. The clock can also be capacitively coupled to the signal source (see Fig. 7). Connecting the internally-generated bias voltage to the clock input, i.e. pin 15 to pin 16 centres the clock input about the switching threshold (see Fig. 8).
2. The two complementary outputs are ECL 10K compatible but internal pulldown resistors are not included, and thus an external resistor to V_{EE} is required. The outputs are capable of driving a 50 ohm load to -2V over the temperature range of 0°C to +70°C. The output high level will typically be reduced by 50mV.
3. The TTL totem pole output operates with the same supply and is powered up by connecting V_{EE} (pin 12) to TTL V_{EE} (pin 13). If the TTL output is not required then the TTL V_{EE} (pin 13) should be left open-circuit reducing the power consumption by 20mW.
4. Both control inputs (PE1 and PE2) are ECL 10K compatible throughout the temperature range. Each control input is provided with a pull up resistor, the remote ends of which are connected to pins 6 and 7. This allows the pull up resistors to be unused if so desired, or to be used to interface from TTL (see Fig. 9). If interfacing to ECL is required then pins 6 and 7 should be left open circuit: alternatively they can be connected to V_{EE} to act as pull-down resistors. When high, the master set input sets the counter to the eleventh state, is asynchronous, and overrides the clock input.
5. All the inputs have an internal pull-down resistor of 50k.
6. The device will operate down to DC but input slew rate must be better than 20V/μs.
7. Input impedance is a function of frequency. See Fig. 5.

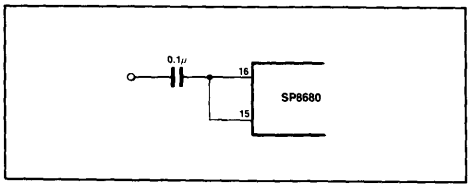


Fig.7 AC coupled input

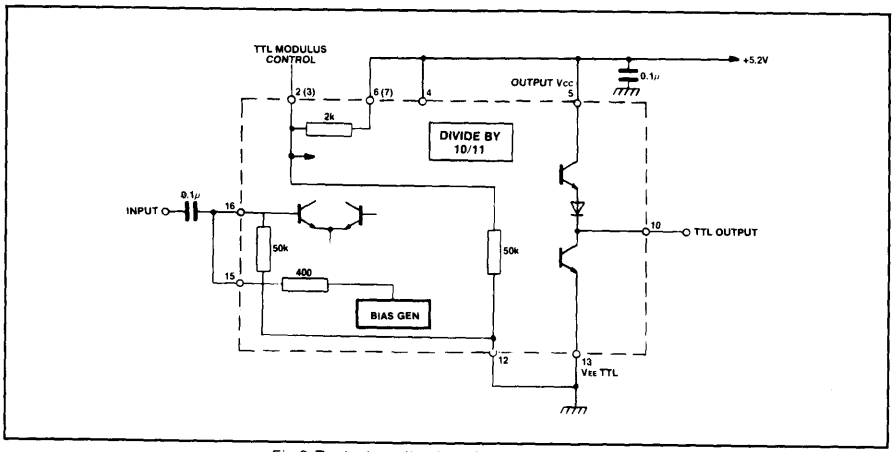


Fig.8 Typical application showing interfacing

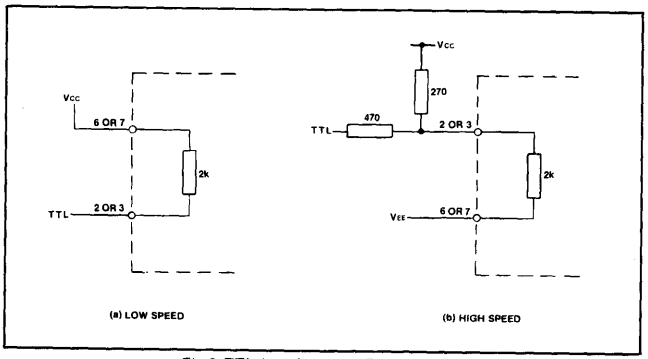


Fig.9 TTL interface to PE1 and PE2

PLESSEY
Semiconductors

SP8685A&B

500MHz ÷ 10/11

The SP8685 is an ECL variable modulus divider, with ECL 10K compatible outputs. It divides by 10 when either of the ECL control inputs, $\overline{PE1}$ or $\overline{PE2}$, is in the high state and by 11 when both are low (or open circuit).

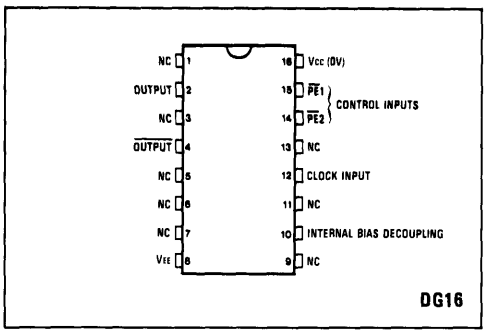


Fig.1 Pin connections - top view

FEATURES

- Divides by 10 and 11
- AC Coupled Input (Internal Bias)
- ECL Compatible Output

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 300mW
- Temperature Range:
  - -55°C to +125°C (A Grade)
  - -30°C to +70°C (B Grade)

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 20mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

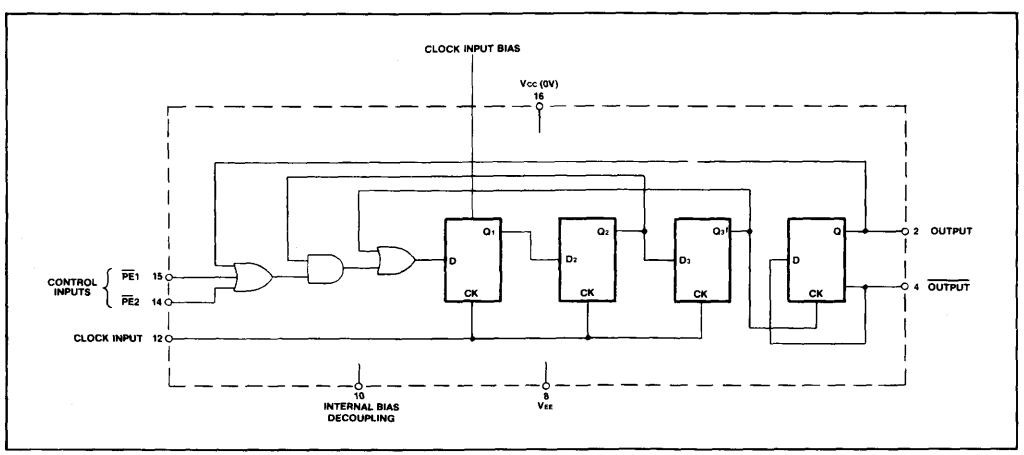


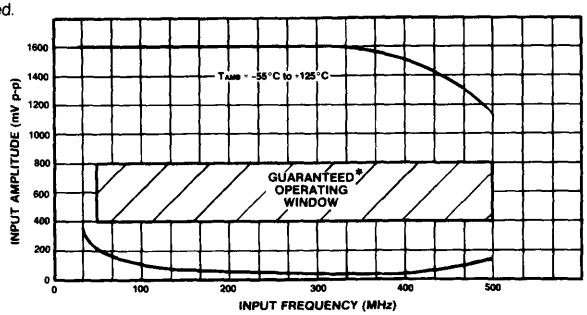
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	500		MHz	Input = 400-800mV p-p	
Minimum frequency (sinewave input)	f_{min}		50	MHz	Input = 400-800mV p-p	Note 6
Power supply current	I_{EE}		70	mA	V_{EE} = -5.2V	Note 6
Output high voltage	V_{OH}	-0.87	-0.7	V	V_{EE} = -5.2V (25°C)	
Output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to output delay	t_p		6	ns		Note 7
Set-up time	t_s	2		ns		Note 7
Release time	t_r	2		ns		Note 7

NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.6.
4. The set up time t_s is defined as minimum time that can elapse between L ⟶ H transition of control input and the next L ⟶ H clock pulse transition to ensure that +10 is obtained.
5. The release time t_r is defined as the minimum time that can elapse between H ⟶ L transition of the control input and the next L ⟶ H clock pulse transition to ensure that the +11 mode is obtained.
6. Tested at 25°C only.
7. Guaranteed but not tested.



*Tested as specified above.

Fig.3 Typical input characteristic SP8685A

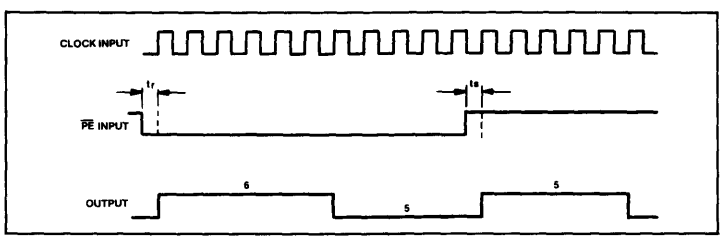


Fig.4 Timing diagram

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from clock input (Pin 12) to V_{EE}. This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig.7.
5. The $\overline{PE}$ inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open.

TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

6. Input impedance is a function of frequency. See Fig. 5.
7. All components should be suitable for the frequency in use.

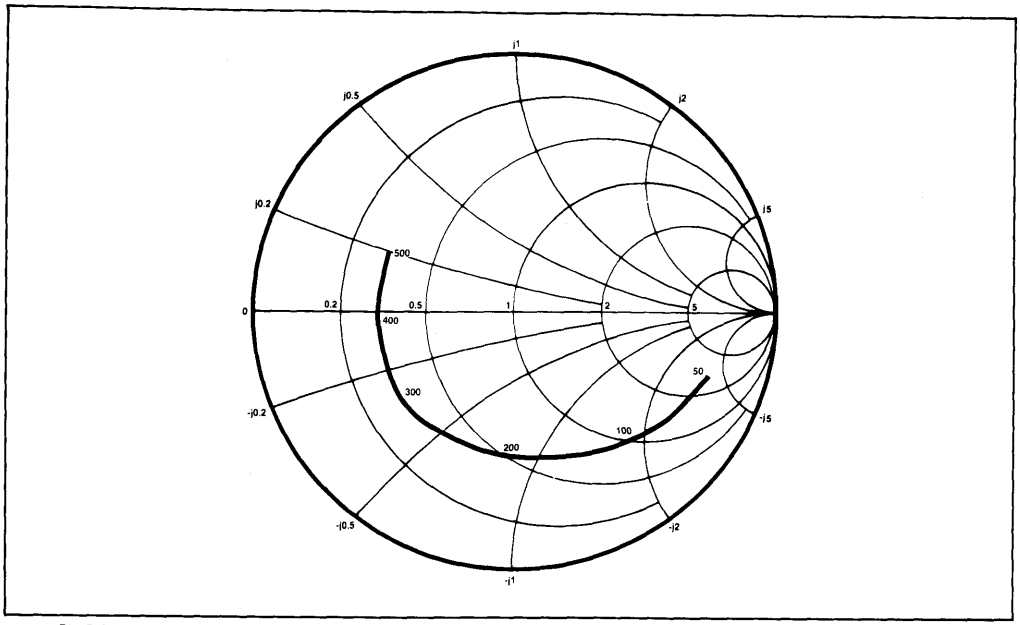


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

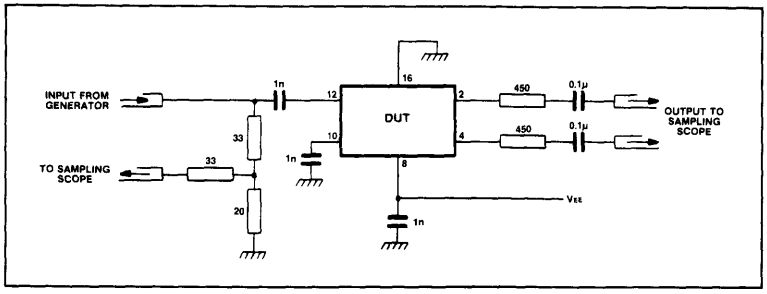


Fig.6 Test circuit

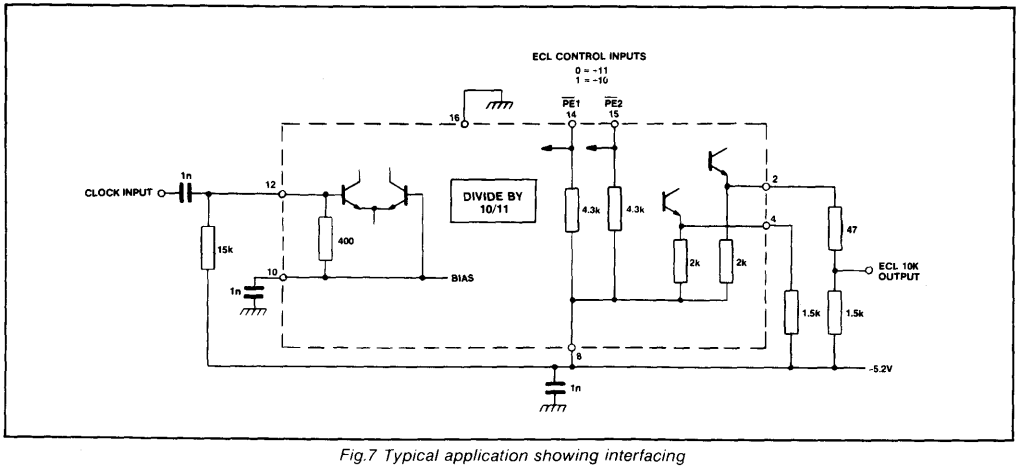


Fig.7 Typical application showing interfacing

PLESSEY
Semiconductors

SP8690A&B 200MHz ÷ 10/11
SP8691A&B 200MHz ÷ 8/9

The SP8690 and SP8691 are low power ECL counters with both ECL 10K and TTL compatible outputs. They divide by the lower division ratio when either control input is in the 'high' state and by the higher ratio when both are 'low' (or open circuit).

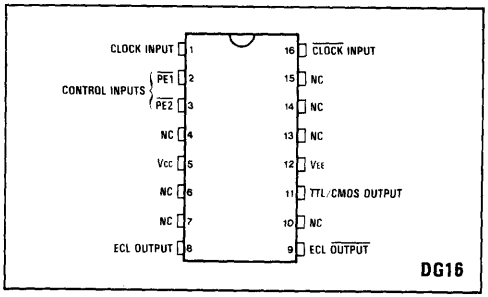


Fig.1 Pin connections - top view

FEATURES

- ECL and TTL/CMOS Output
- AC Coupled Input
- Control Inputs ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 70mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Output ECL Current: 10mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- TTL Output: +12V
- Input Voltage: 2.5V p-p
- Max. Open Collector Current: 15mA

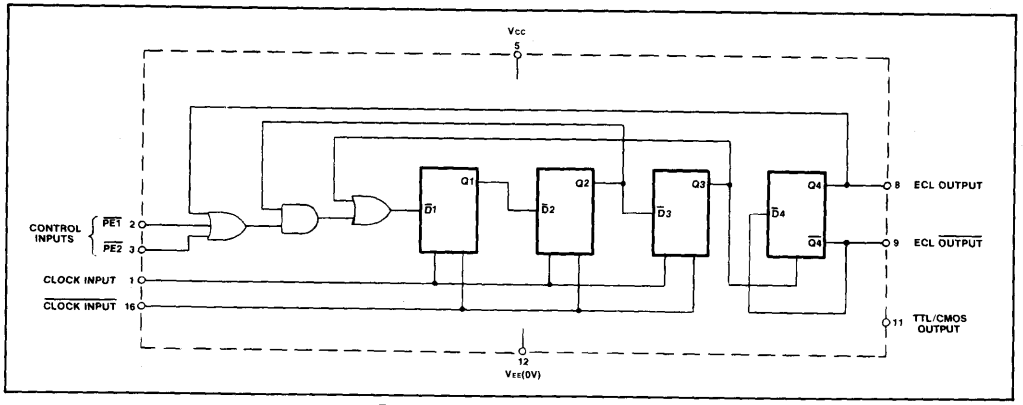


Fig.2 Functional diagram (SP8690)

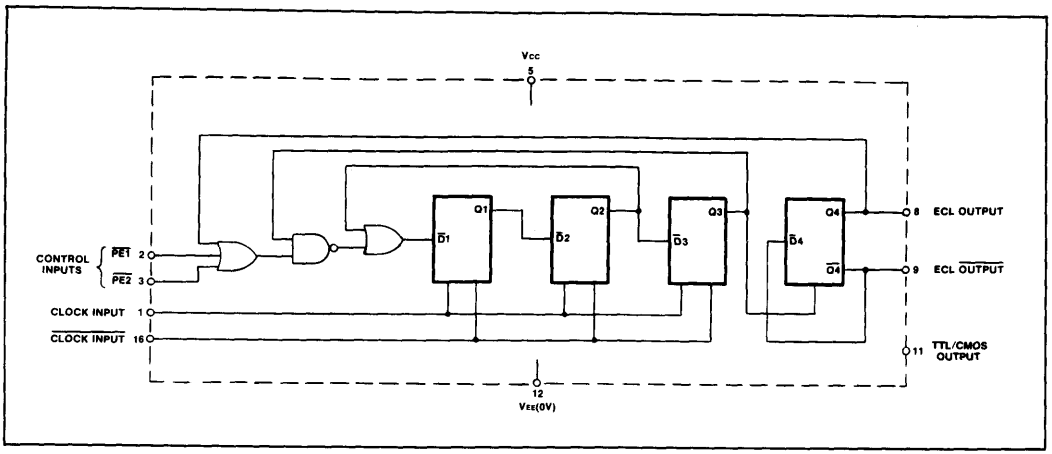


Fig.3 Functional diagram (SP8691)

ELECTRICAL CHARACTERISTICS

TTL OPERATION

Supply Voltage: V_{CC} = 5.0 ± 0.25V V_{EE} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input =400 - 800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input =400 - 800mV p-p	Note 3
Power supply current	I_{EE}		21	mA	V_{CC}= 5.0V	Note 3
TTL output high voltage	V_{OH}	3.75		V	V_{CC} = 5V RL = 560Ω	Note 3, 5
TTL output low voltage	V_{OL}		0.5	V	RL = 560Ω	Note 3, 5
Clock to TTL output delay (positive going)	t_{pLH}		32	ns	RL = 560Ω	Note 4
Clock to TTL output delay (negative going)	t_{pHL}		18	ns	RL = 560Ω	Note 4
Set-up time	t_s		3	ns		Note 4
Release time	t_r		8	ns		Note 4

NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8690/1B tested at 25°C only.
4. Guaranteed but not tested.
5. Open collector output not recommended for use above 15MHz output frequency. $C_{load} \leqslant 5pF$.

ELECTRICAL CHARACTERISTICS

ECL OPERATION

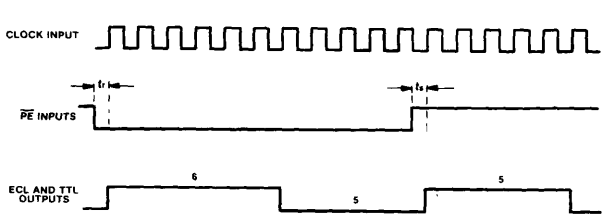
Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		21	mA	V_{EE} = -5.0V	Note 3

ELECTRICAL CHARACTERISTICS (CONTINUED)
ECL OPERATION

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V(25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V(25° C)	
PE input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V(25° C)	
PE input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V(25° C)	
Clock to ECL output delay	t_p		9	ns		Note 4
Set-up time	t_s	3		ns		Note 4
Release time	t_r	8		ns		Note 4

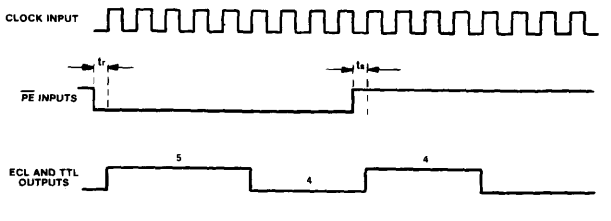
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8690/1B tested at 25°C only.
4. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Fig.4 Timing diagram SP8690

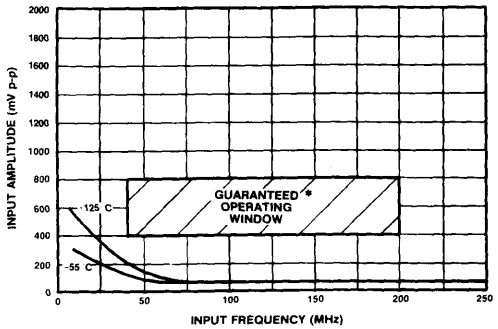


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	9
H	L	8
L	H	8
H	H	8

Fig.5 Timing diagram SP8691

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷10 or 8 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷11 or 9 mode is obtained.



*Tested as specified above.

Fig.6 Typical input characteristics SP86790/1

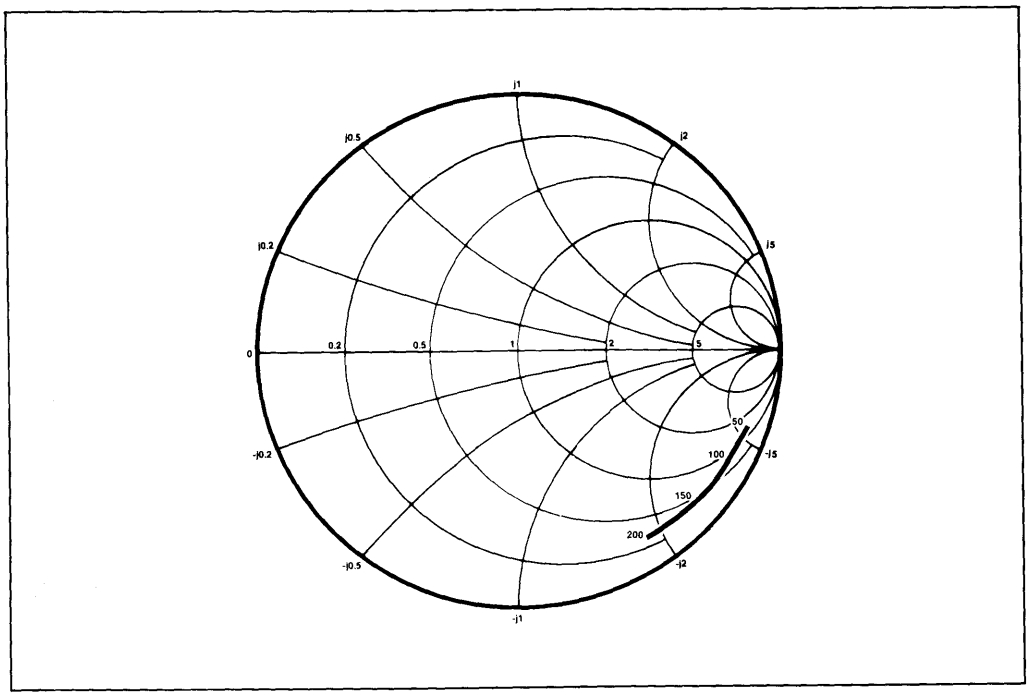


Fig.7 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs can be single or differentially driven. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. In the absence of a signal the device will self-oscillate. If this is undesirable it may be prevented by connecting a 68k resistor from the input to V_{EE} (i.e. Pin 1 or 16 to Pin 12). This reduces input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/µs.
4. The Q_4 and $\overline{Q_4}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 9.
5. The PE inputs are ECL III/10K compatible and include a 10k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8690/1 varies as a function of frequency. See Fig. 7.
7. The TTL/CMOS output has a free collector and the high state output voltage will depend on the supply that the collector load is taken too. This should not exceed 12V.
8. The rise/fall time of the open collector output waveform is directly proportional to load capacitance and load resistor value. Therefore load capacitance should be minimised and the load resistor kept to a minimum compatible with system power requirements. In the test configuration of Fig.8 the output rise time is approximately 10ns and fall time is 7ns typically.

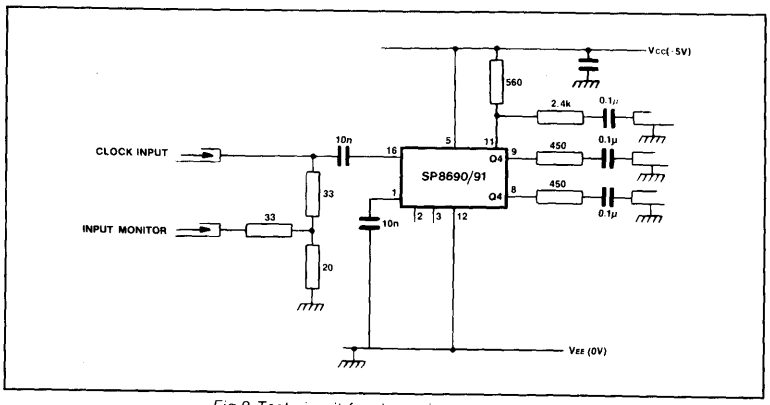


Fig.8 Test circuit for dynamic measurements

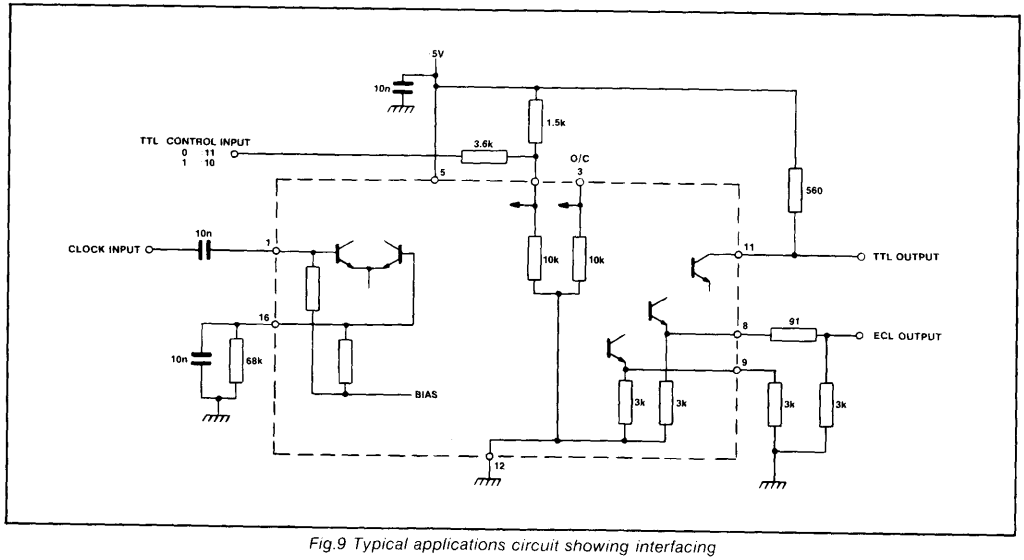


Fig.9 Typical applications circuit showing interfacing

PLESSEY
Semiconductors

SP8695A&B

200MHz ÷ 10/11

The SP8695 is a low power ECL counter with both ECL 10K and TTL compatible outputs. They divide by 10 when either control input in the 'high' state and by 11 when both are 'low' (or open circuit). The inputs are ECL II compatible but can also be AC coupled. An open collector output is provided for interfacing to TTL or CMOS.

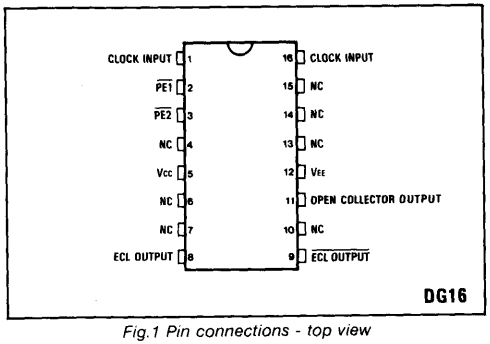


Fig.1 Pin connections - top view

FEATURES

- Low Frequency Operation
- ECL and TTL/CMOS Outputs
- DC or AC Coupled Input
- Temperature Ranges:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

QUICK REFERENCE DATA

- Supply Voltage: +5.0V
- Power Consumption: 80mW
- Maximum Input Frequency: 200MHz

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Output ECL Current: 10mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Input Voltage: 2.5V p-p
- Max. Open Collector Output Voltage: +12V
- Max. Open Collector Current: 15mA

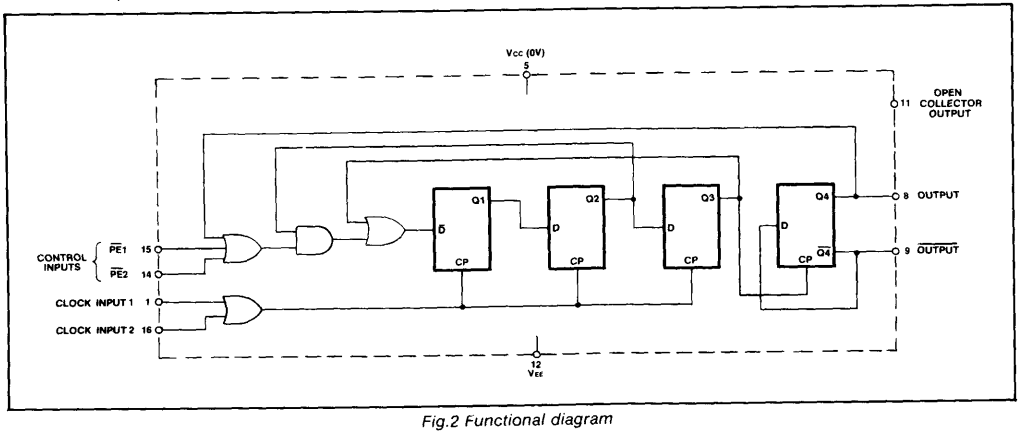


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

ECL OPERATION

Supply Voltage: V_{EE} = -5.2V ± 0.25V V_{CC} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade: T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Temperature
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		2	MHz	Input = 400-800mV	Note 4
Power supply current	I_{EE}		21	mA	V_{EE} = -5.0V	Note 3
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25° C)	
ECL output high voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25° C)	
PE input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25° C)	
PE input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25° C)	
Clock to ECL output delay	t_p		9	ns		Note 4
Set-up time	t_s	3		ns		Note 4
Release time	t_r	8		ns		Note 4

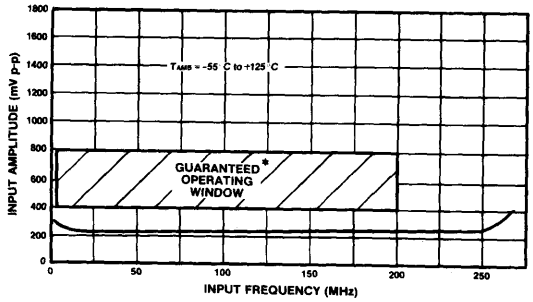
NOTES
1. Unless otherwise stated, the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8695B tested at 25°C only.
4. Guaranteed but not tested.
5. TTL output not recommended for use above 15MHz output frequency. $C_{load} \leq$ 5pF.

ELECTRICAL CHARACTERISTICS

TTL OPERATION

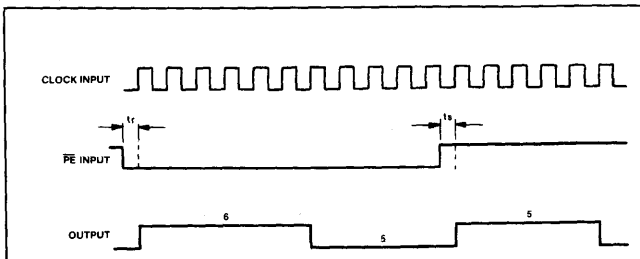
Supply Voltage: V_{CC} = 5.0 ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	200		MHz	Input =400 - 800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		2	MHz	Input =400 - 800mV p-p	Note 4
Power supply current	I_{EE}		21	mA	V_{CC}= 5.0V	Note 3
TTL output high voltage	V_{OH}	3.75		V	V_{CC}= 5V RL = 560Ω	Note 3, 5
TTL output low voltage	V_{OL}		0.5	V	RL = 560Ω	Note 3
Clock to TTL output delay (positive going)	t_{pLH}		32	ns	RL = 560Ω	Note 4
Clock to TTL output delay (negative going)	t_{pHL}		18	ns	RL = 560Ω	Note 4
Set-up time	t_s	3		ns		Note 4
Release time	t_r	8		ns		Note 4



*Tested as specified above.

Fig.3 Typical input characteristics SP8695A



CONTROL INPUT TRUTH TABLE

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	11
H	L	10
L	H	10
H	H	10

Fig.4 Timing diagram SP8695

NOTES

The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure that the ÷10 mode is obtained.

The release time t_r is defined as the minimum time that can elapse between a H→L transition of control input and the next L→H clock pulse transition to ensure that the ÷11 mode is obtained.

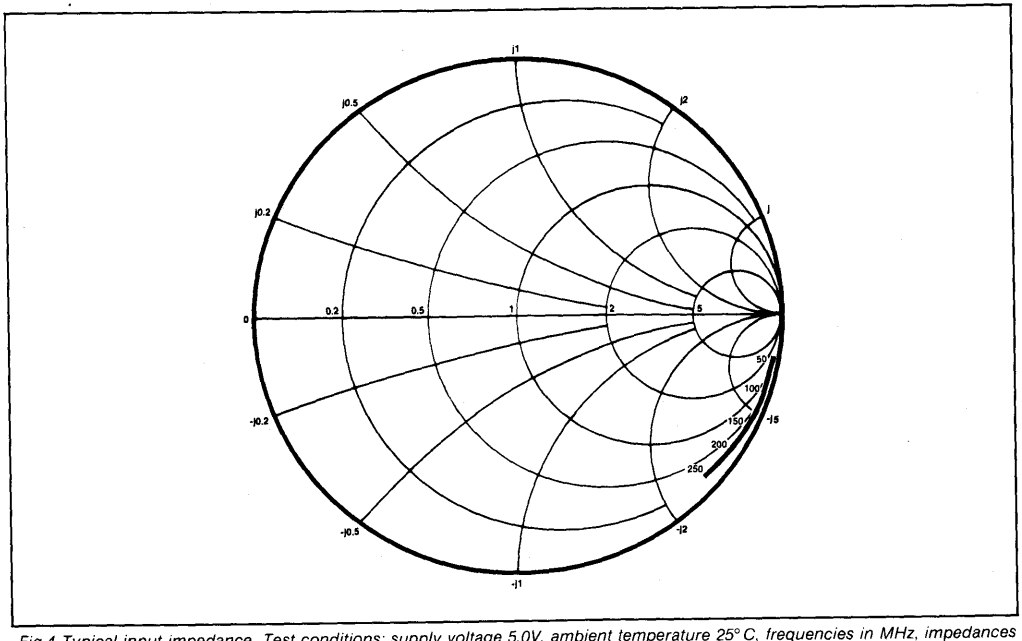


Fig.4 Typical input impedance. Test conditions: supply voltage 5.0V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock inputs can be driven from ECL II, III and 10K. The input reference voltage (-3.8V at 25°C) is compatible with ECL II, III and 10K over the specified temperature range. The inputs can also be capacitively coupled by addition of external bias as shown in Fig. 6. Each input has an internal pull-down resistor of 10k, and unused inputs can therefore be left open circuit. They should by bypassed to RF where maximum noise immunity is required.
2. The PE control inputs are similarly ECL III/10K compatible and also have an internal 10k pull-down resistor, allowing unused inputs to be left open circuit if required.
3. The Q_4 and $\overline{Q_4}$ ECL outputs have internal circuitry equivalent to a 14k pull-down resistor on each output and are ECL II compatible: they can however be interfaced to ECL III/10K as shown in Fig. 8.
4. The circuit will operate down to DC but slew rate must be better than 5V/µs.
5. The input impedance of SP8695 varies as a function of frequency. See Fig. 5.
6. The TTL/CMOS output has a free collector and the high state output voltage will depend on the supply that the collector load is taken to. This should not exceed 12V. The rise and fall time of the open collector output waveform is directly proportional to load capacitance and load resistance value. Therefore load capacitance should be kept to a minimum and the load resistor kept to a minimum compatible with system power requirem In the test configuration of Fig. 6 the output rise time is oximately 10ns and fall time is 7ns typically.

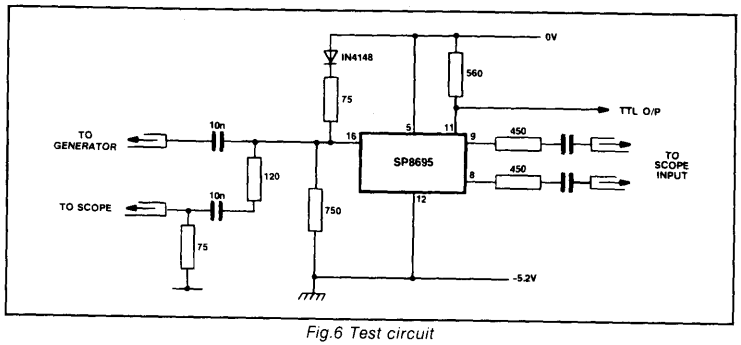


Fig.6 Test circuit

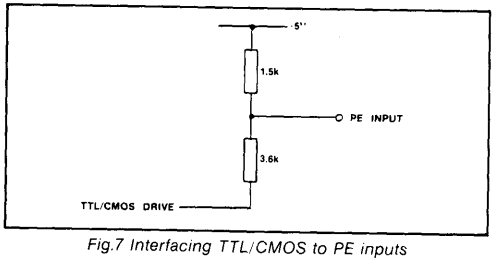


Fig.7 Interfacing TTL/CMOS to PE inputs

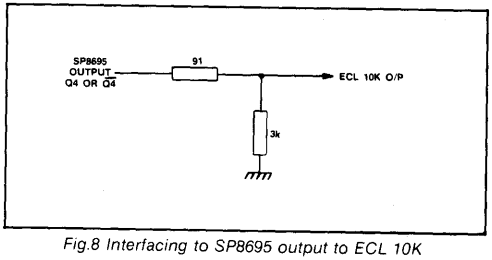


Fig.8 Interfacing to SP8695 output to ECL 10K

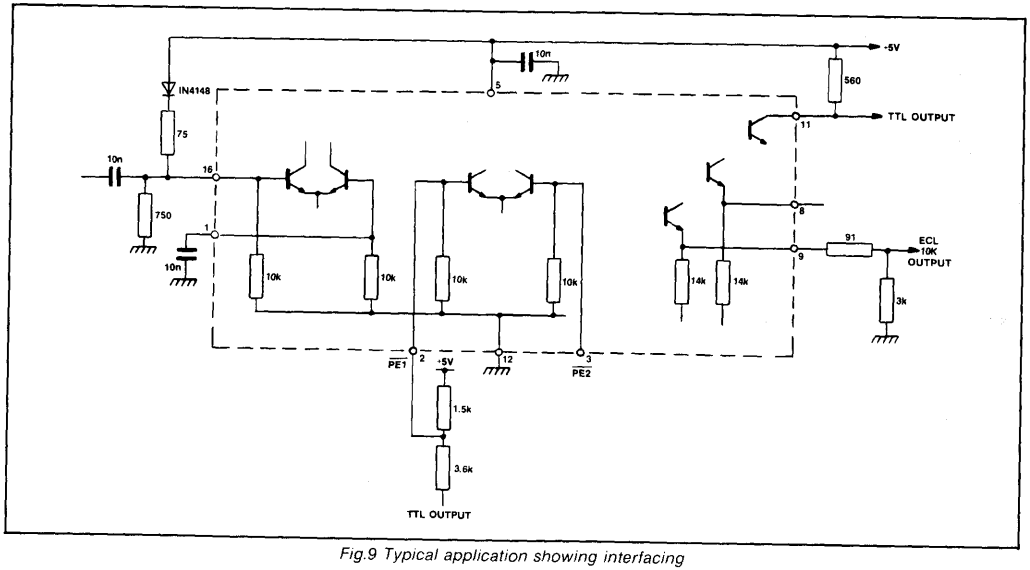


Fig.9 Typical application showing interfacing

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PLESSEY
Semiconductors

SP8703

1GHz LOW CURRENT TWO-MODULUS DIVIDER

The SP8703 is a divide by 128/9 programmable divider with a maximum specified operating frequency of 1GHz.

The signal (clock) inputs are biased internally and require to be capacitor coupled.

The output stage is CMOS compatible only, the 0 to 1 output edge giving maximum loop delay.

A unique 'power-down' feature is included to minimise power consumption.

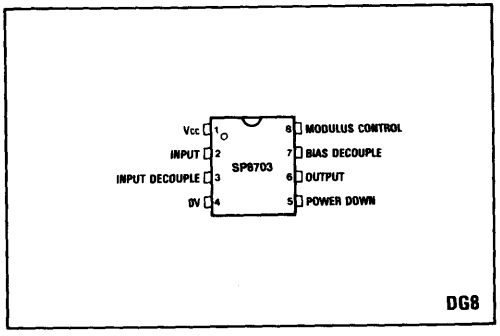


Fig.1 Pin connections - top view

FEATURES

- DC to 1GHz Operation
- -30° to +70°C Temperature Range
- Unique Power-Down Feature
- CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.0V ± 0.25V
- Supply Current 30mA Typical

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 6V
- Storage Temperature Range: -30°C to +150°C
- Junction Temperature: +175°C
- Input Voltage: 2.5V p-p

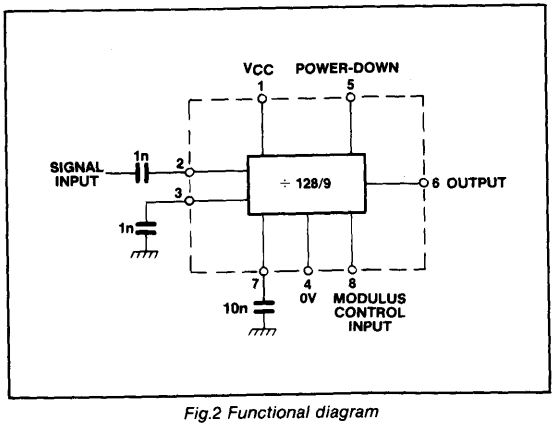


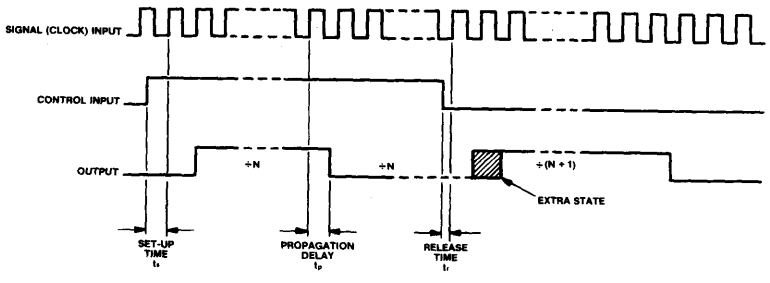
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{CC} = +4.75V to 5.25V, T_{amb} = -30°C to +70°C

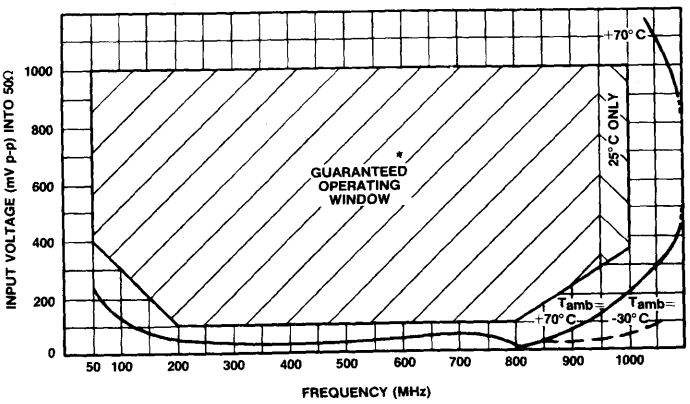
Characteristics	Value		Units	Conditions	Notes
	Min.	Max.			
Maximum frequency	1000		MHz	T_{amb} = 25°C	Note 1,2,4
Maximum frequency	950		MHz		Note 1,2,3
Minimum frequency (sinewave)		50	MHz		Note 1,2,3
Power supply current		40	mA	Power-up	Note 3
Power supply current		3	mA	Power-down	Note 3
Output high voltage	3.2	V_{CC}	V	IL = -0.2mA	Note 3
Output low voltage	0	1.7	V	IL = 0.2mA	Note 3
Control input high voltage	3.2	V_{CC}	V	Divide by 128	Note 3
Control input low voltage	0	1.7	V	Divide by 129	Note 3
Control input high current		50	μA	Input = V_{CC}	Note 3
Control input low current	-10		μA	Input = 0V	Note 3
Power-down high voltage	3.2	V_{CC}	V	Power-down	Note 3
Power-down low voltage	0	1.7	V	Power-up	Note 3
Power-down high current		10	μA	Input = V_{CC}	Note 3
Power-down low current	-2		μA	Input = 0V	Note 3
Clock to output delay		30	ns	CL = 10pF	Note 5
Set-up time		15	ns	CL = 10pF	Note 5
Release time		15	ns	CL = 10pF	Note 5

NOTES
1. See Fig.4 for guaranteed operating window.
2. See Fig.5 for input voltage measurement method.
3. Tested at 25°C and +70°C only.
4. Tested at 25°C only.
5. Guaranteed but not tested.



NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷N mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷(N + 1) mode is obtained.

Fig.3 Timing diagram



*Tested as specified above.

Fig.4 Typical input characteristics

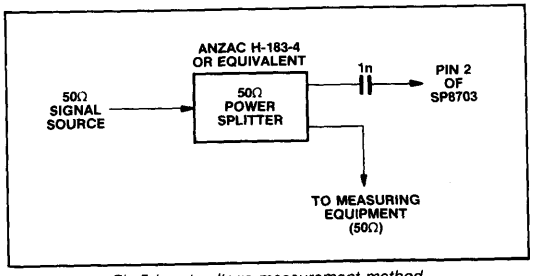


Fig.5 Input voltage measurement method

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/μs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.

PLESSEY
Semiconductors

SP8712B

2400MHz ÷ 4

The SP8712B is an asynchronous emitter coupled logic counter which provides ECL 10K compatible outputs and can drive 100 ohm lines. It operates from a -6.8V supply or split supplies of +5V and -1.8V. Otherwise it is similar to the SP8610 and SP8611.

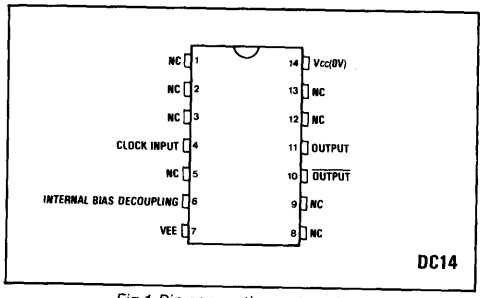


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Output
- AC Coupled Input (Internal Bias)
- Typical Operating Frequency 2.5GHz

QUICK REFERENCE DATA

- Supply Voltage: -6.8V
- Power Consumption: 630mW typ.
- Output Voltage Swing 800mV typ.

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage (V_{CC} - V_{EE}) = 8V
- Output Current: 15mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Input Voltage: 2.5V p-p

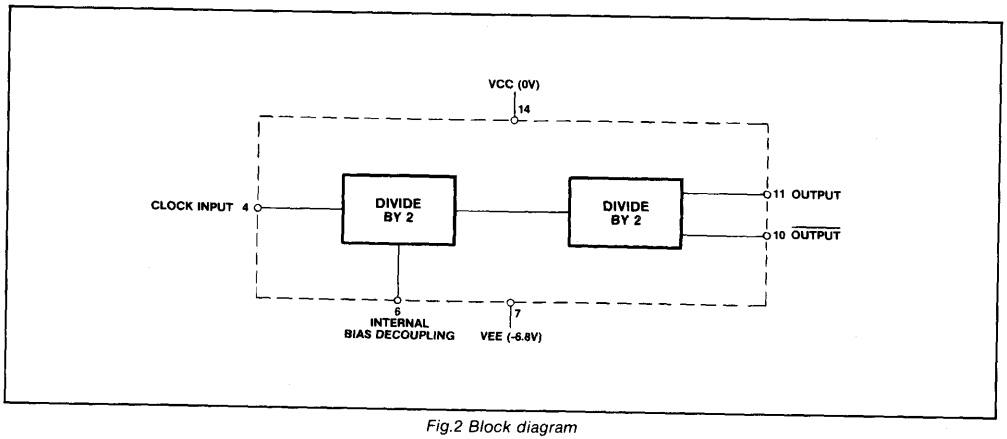


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} = 0V, V_{EE} = -6.8V ± 0.35V
Temperature: T_{amb} = 0°C to +70°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	2.4		GHz	Input = 600mV pk-pk	Note 4
Minimum frequency sinewave input	f_{min}		500	MHz	Input = 400mV pk-pk	Note 5
Power supply current	I_{EE}		110	mA	Outputs unloaded V_{EE} = -7.15V	Note 5
Output low voltage	V_{OL}	-0.93	-0.7	V	Outputs loaded with 620Ω to V_{EE} = -6.8V (25°C)	
Output high voltage	V_{OH}	-1.9	-1.6	V	Outputs loaded with 620Ω to V_{EE} = -6.8V (25°C)	
Minimum output swing	V_{OUT}	0.7		V	Outputs loaded with 620Ω to V_{EE} = -6.8V	Note 5

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.2mV/°C and V_{OL} = +0.24mV/°C but these are not tested.
3. The test configuration for dynamic testing is shown in Fig.5.
4. Tested at +70°C only.
5. Tested at 25°C only.

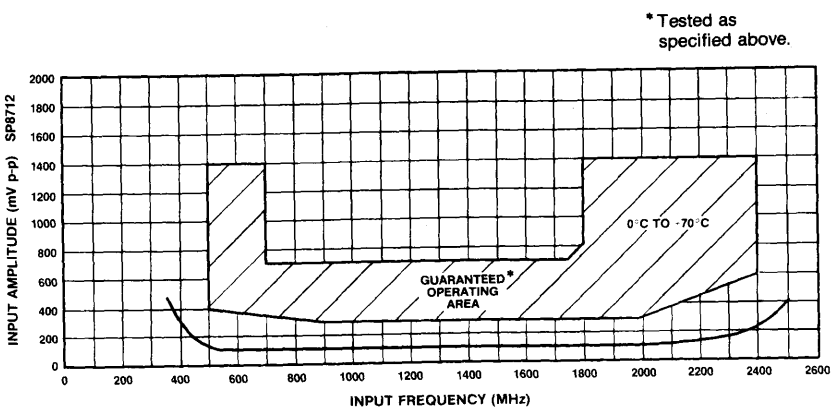


Fig.3 Typical input characteristics SP8712

OPERATING NOTES

1. The clock input (pin 4) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling pin (6) to ground.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the input to V_{EE} (i.e. pin 4 to pin 7). This reduces sensitivity by approximately 100mV.
3. The input can be operated at very low frequencies but slew rate must be better than 200V/μs.
4. The input impedance of the SP8712 is a function of frequency. See Fig.4.
5. The emitter follower outputs require external load resistors. These should not be less than 330 ohms, and a value of 620 ohms is recommended. Interfacing to ECL III/10K is shown in Fig.7.
6. These devices may be used with split supply lines by means of the circuit of Fig.6. Some improvement in the upper frequency of operation may be obtained under these conditions, but suitable circuit layout must be employed to achieve this improvement.
7. To obtain the best performance from these devices, good RF construction techniques must be employed: the use of leadless chip capacitors is recommended.

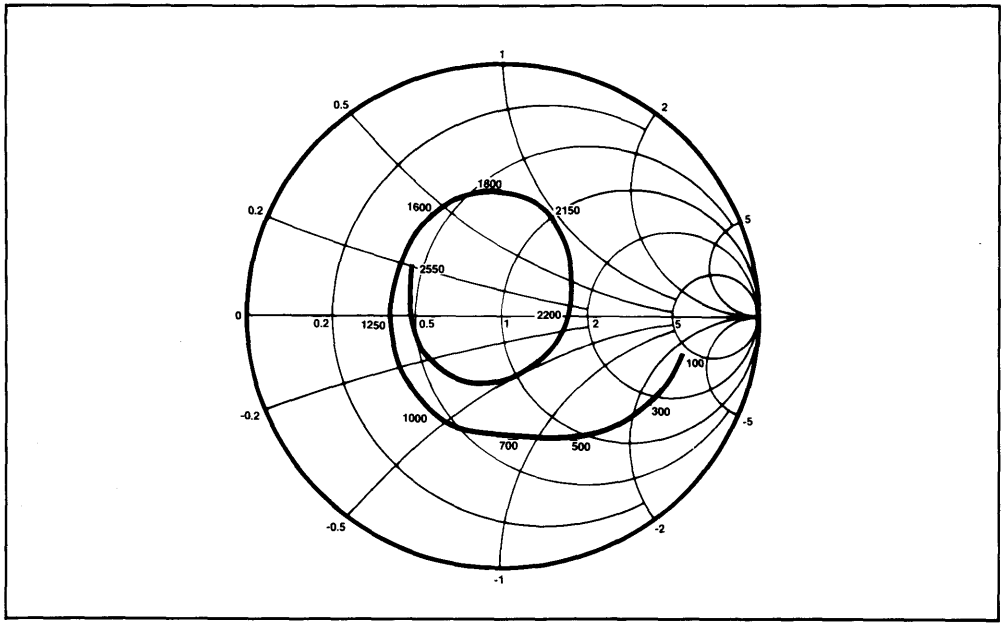


Fig.4 Typical input impedance. Test conditions: supply voltage -6.8V, ambient temperature 25°C. Frequencies in MHz, impedances normalised to 50 ohms.

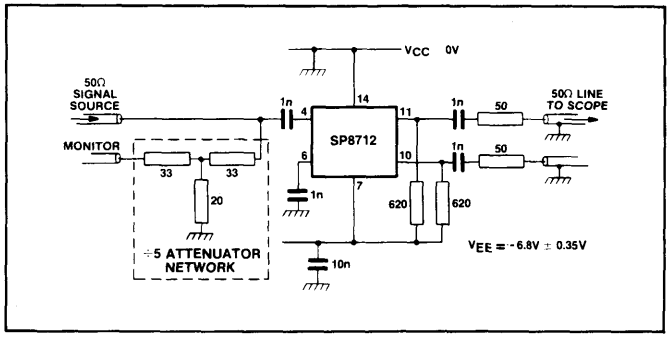


Fig.5 Toggle frequency test circuit

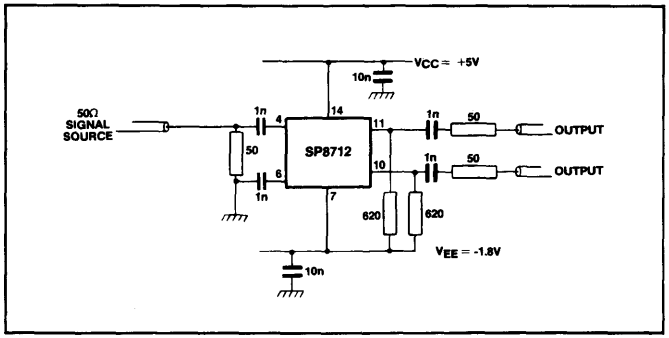


Fig.6 Operation on split supply voltages

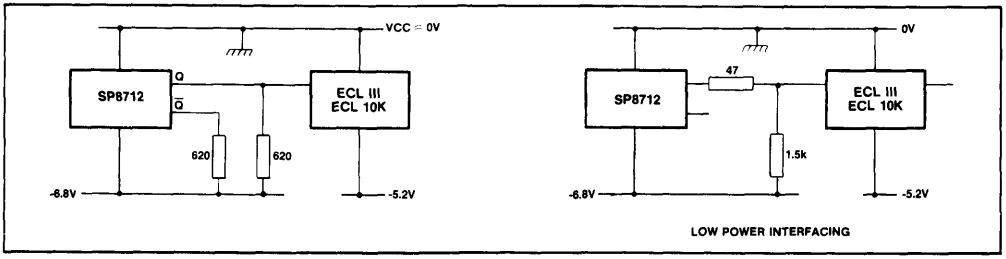


Fig.7 Interfacing SP8712 series to ECL 10K and ECL III

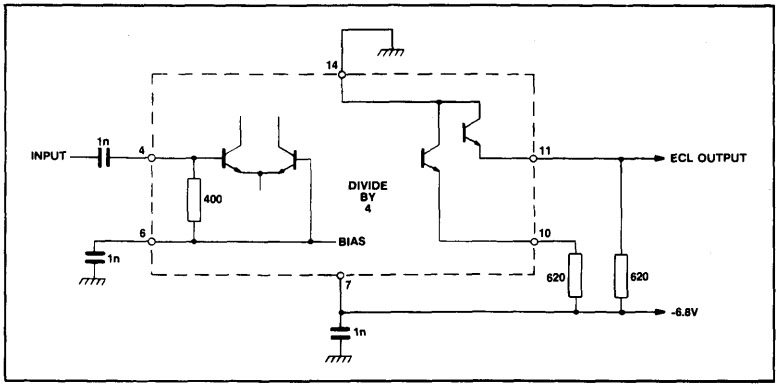


Fig.8 Typical application showing interfacing

PLESSEY
Semiconductors

SP8716/8/9

520MHz ULTRA LOW CURRENT TWO MODULUS DIVIDERS

SP8716 ÷ 40/41, SP8718 ÷ 64/65, SP8719 ÷ 80/81 are 50mW programmable dividers with a maximum specified operating frequency of 520MHz over the temperature range -30°C to +70°C.

The signal (clock) inputs are biased internally and require to be capacitor coupled. The output stage is of an unusual low power design featuring dynamic pull-up, and optimised for driving CMOS. The 0 to 1 output edge should be used to give the best loop delay performance.

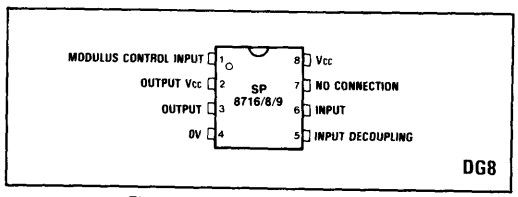


Fig.1 Pin connections - top view

FEATURES

- DC to 520MHz Operation
- -40°C to +85°C Temperature Range
- Control Inputs and Outputs are CMOS Compatible

QUICK REFERENCE DATA

- Supply Voltage 5.2V ± 0.25V
- Supply Current 10.5mA typ.

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage (Pin 2 or 8): 8V
- Storage Temperature Range: -40°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

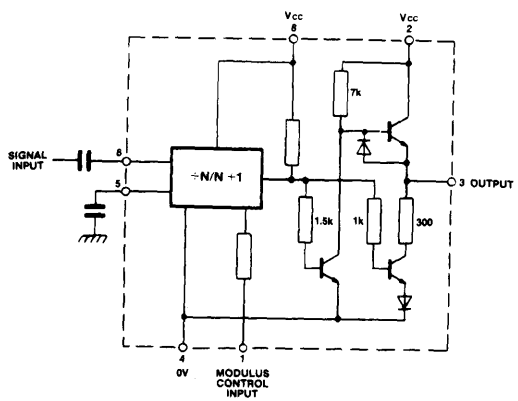


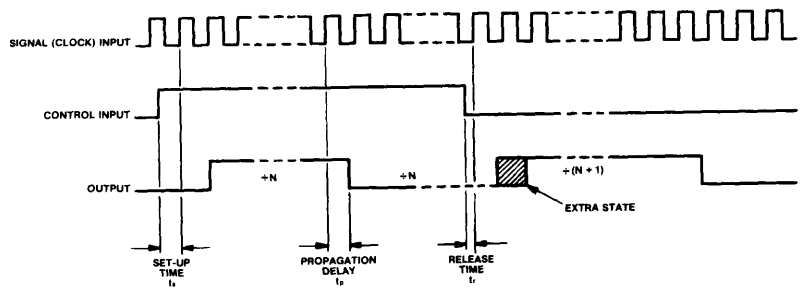
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Supply voltage: V_{CC} = +4.95 to 5.45V, Temperature: T_{amb} = -40°C to +85°C

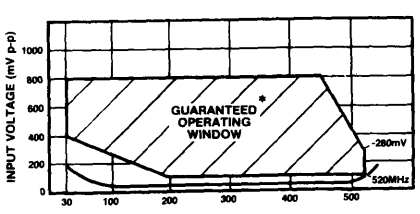
Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Max. frequency	f_{max}	520		MHz	Input 100-280mV p-p	1
Min. frequency (sinewave input)	f_{min}		30	MHz	Input 400-800mV p-p	2
Power supply current	I_{CC}		11.9	mA	C_L = 3pF; pins 2, 8 linked	1
Output high voltage	V_{OH}	(V_{CC} -1.2)		V	I_L = -0.2mA	1
Output low voltage	V_{OL}		1	V	I_L = 0.2mA	1
Control input high voltage	V_{INH}	3.3	8	V	÷N	1
Control input low voltage	V_{INL}	0	1.7	V	÷N + 1	1
Control input high current	I_{INH}		0.41	mA	V_{INH} = 8V	1
Control input low current	I_{INL}	-0.20		mA	V_{INL} = 0V	1
Clock to output delay	t_p		28	ns	C_L = 10pF	2
Set-up time	t_s	10		ns	C_L = 10pF	2
Release time	t_r	10		ns	C_L = 10pF	2

NOTES
1. Tested at 25°C only.
2. Guaranteed but not tested.



NOTE
The set-up time t_s is defined as the minimum time that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷N mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷(N + 1) mode is obtained.

Fig.3 Timing diagram



*Tested as specified above.

Fig.4 Typical input characteristics

OPERATING NOTES

1. The inputs are biased internally and coupled to a signal source with suitable capacitors.
2. If no signal is present the devices will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from one input to pin 4 (ground). This will reduce the sensitivity.
3. The circuits will operate down to DC but slew rate must be better than 100V/µs.
4. The output stage is of an unusual design and is intended to interface with CMOS. External pull-up resistors or circuits must not be used.
5. This device is NOT suitable for driving TTL or its derivatives.

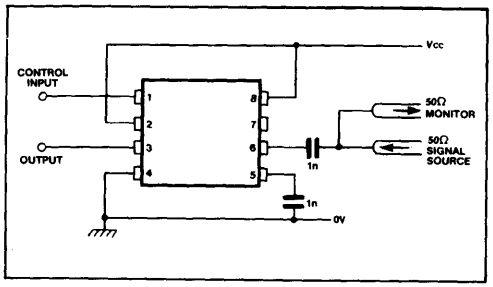


Fig.5 Toggle frequency test circuit

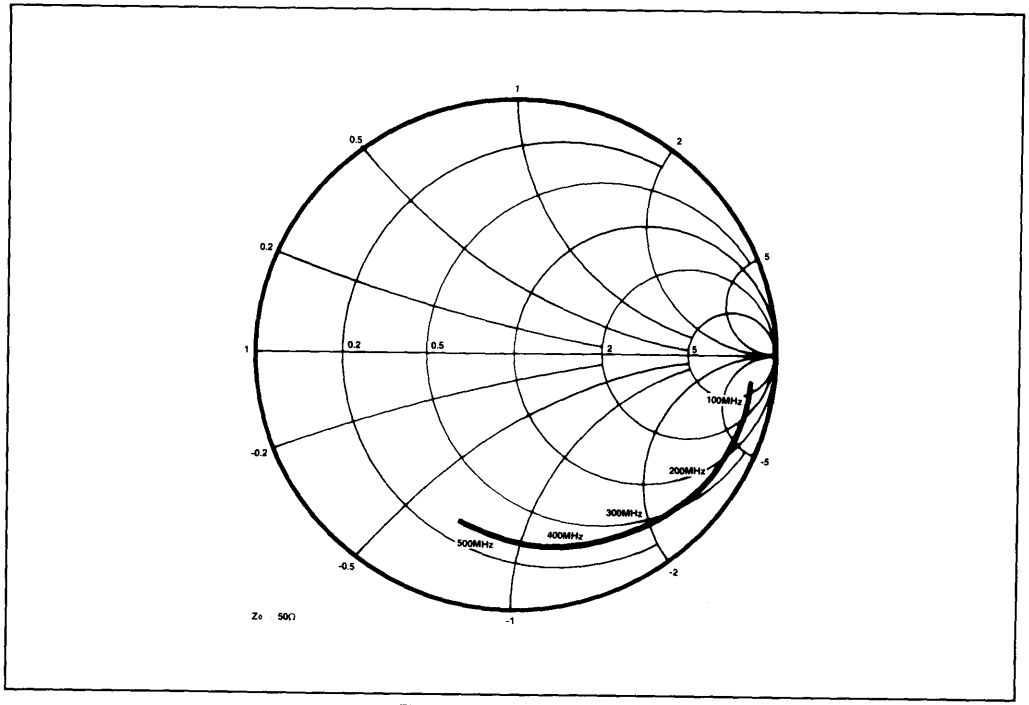


Fig.6 Typical input impedance

PLESSEY
Semiconductors

SP8720A&B

300MHz ÷ 3/4

The SP8720 is an ECL counter with ECL 10K compatible outputs. It divides by 3 when either control input is in the high state and by 4 when both inputs are low (or open circuit). An AC coupled input of 600mV p-p is required.

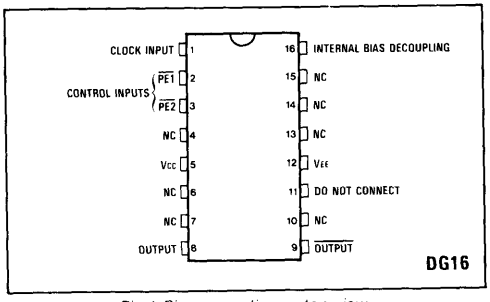


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Input (Internal Bias)
- Control Inputs ECL III/10K Compatible

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 20mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

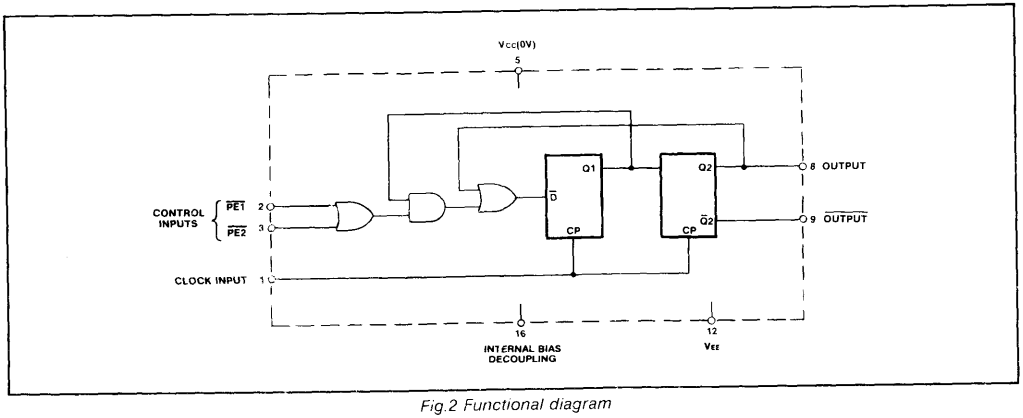


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

ECL OPERATION

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V

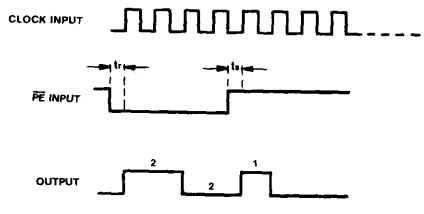
Temperature: A Grade T_{amb} = -55°C to +125°C

B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Conditions	Notes
Maximum frequency sinewave input	f_{max}	300		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		65	mA	V_{EE} = -5.2V	Note 3
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input high voltage	V_{INH}	-0.93		V	V_{EE} = -5.2V (25°C)	
$\overline{PE}$ input low voltage	V_{INL}		-1.62	V	V_{EE} = -5.2V (25°C)	
Clock to ECL output delay	t_p		6	ns		Note 4
Set-up time	t_s		2.5	ns		Note 4
Release time	t_r		3	ns		Note 4

NOTES

1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C but these are not tested.
3. SP8720B tested at 25°C only.
4. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

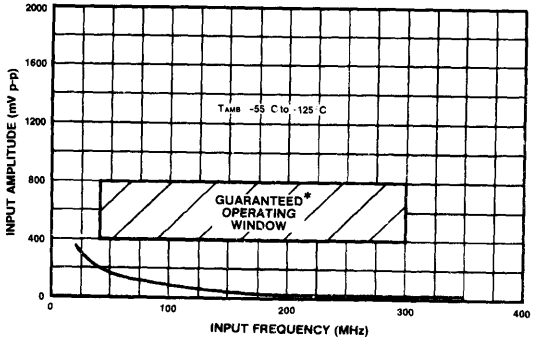
$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	4
H	L	3
L	H	3
H	H	3

Fig.3 Timing diagram

NOTE:

The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷3 mode is obtained.

The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷4 mode is obtained.



*Tested as specified above.

Fig.4 Typical input characteristics SP8720A

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The Q and $\overline{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2k pulldown resistor at each output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8720 varies as a function of frequency. See Fig. 5.

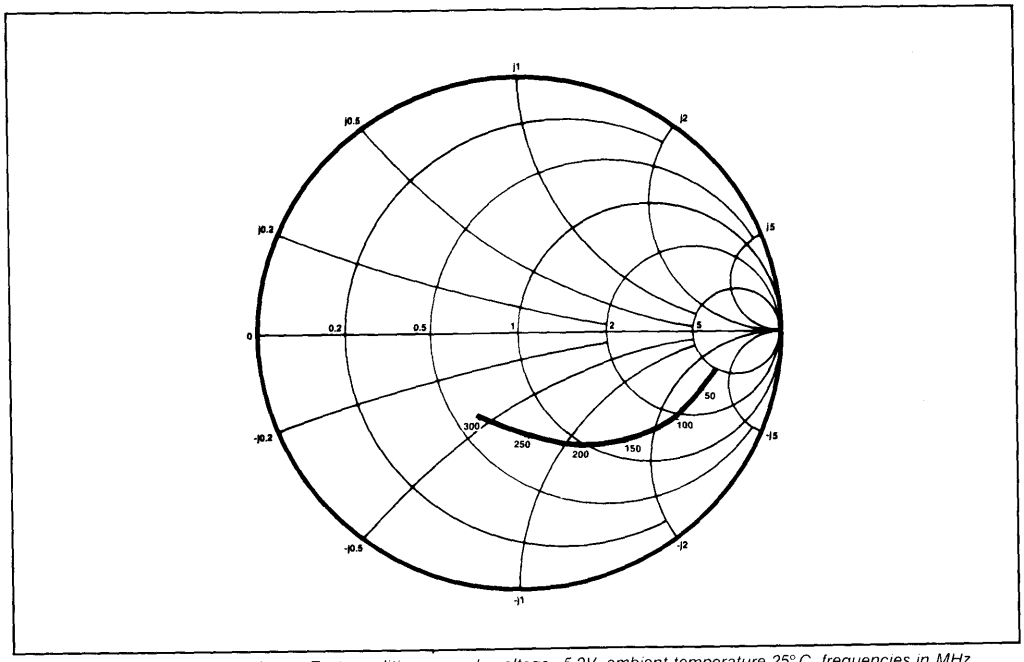


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

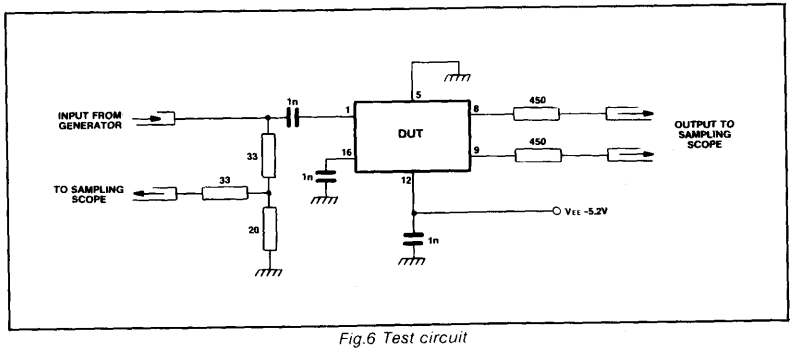


Fig.6 Test circuit

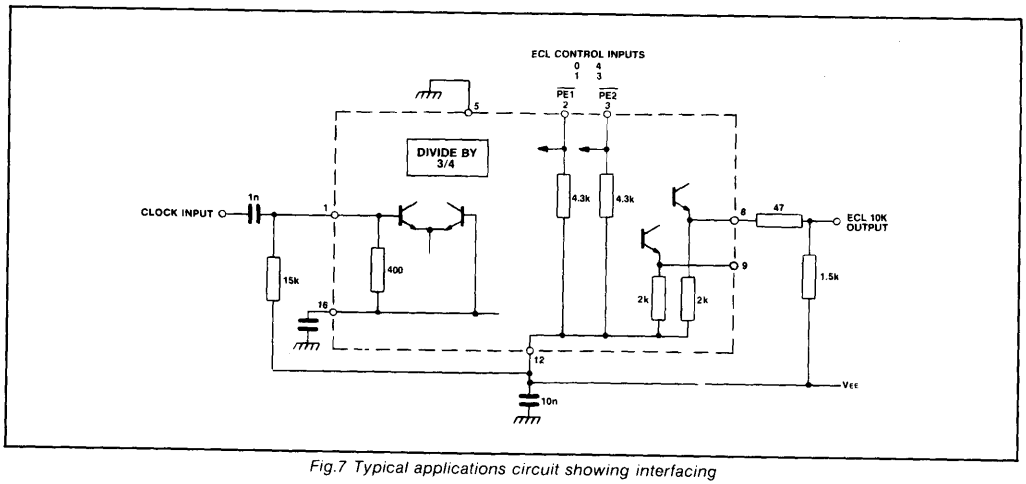


Fig.7 Typical applications circuit showing interfacing

PLESSEY
Semiconductors

SP8735B

600MHz ÷ 8 (BINARY OUTPUTS)

The SP8735 is an ECL counter with binary outputs. In addition, carry outputs are provided in TTL and ECL. The AC coupled input requires 600mV p-p, and the outputs are open collectors. A TTL compatible reset is provided, making this device ideal for instrumentation applications.

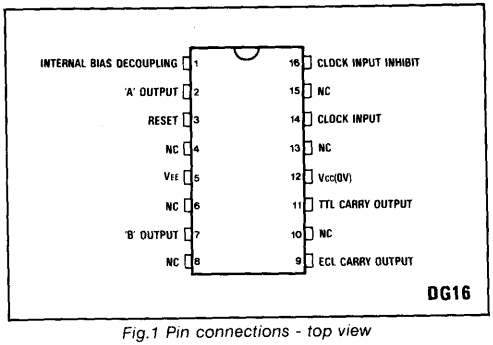


Fig.1 Pin connections - top view

FEATURES

- Binary Outputs to Open Collectors
- Reset Input TTL Compatible
- AC Coupled Input
- Clock Inhibit ECL Compatible
- TTL and ECL Compatible Carry Outputs

QUICK REFERENCE DATA

- Supply Voltage: 5.2V
- Power Consumption: 400mW
- Temperature Range: 0 to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Binary Output Voltage: VEE +11V
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

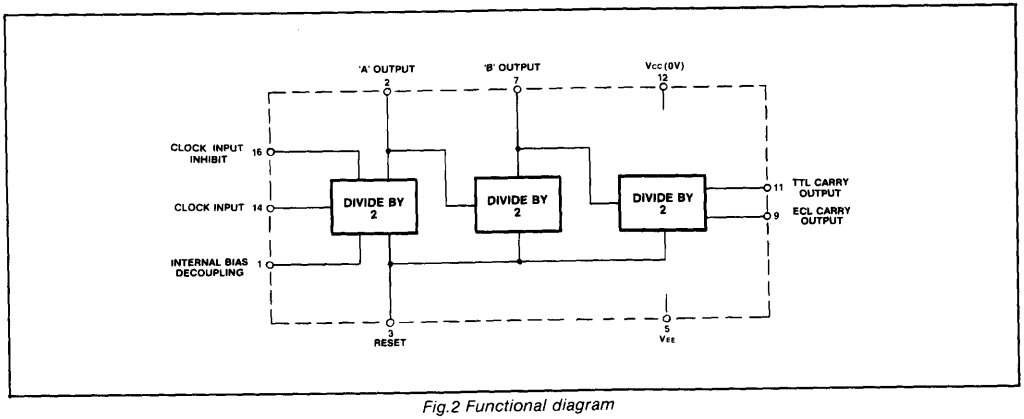


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: T_{amb} = 0°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	600		MHz	Input = 400-800mV p-p	Note 5
Minimum frequency (sinewave input)	f_{min}		40	MHz	Input = 400-800mV p-p	Note 7
Power supply current	I_{EE}		90	mA	V_{EE} = -5.2V	Note 6
Clock inhibit high voltage	V_{INH}	-0.96		V	V_{EE} = -5.2V (25°C)	
Clock inhibit low voltage	V_{INL}		-1.65	V	V_{EE} = -5.2V (25°C)	
TTL output high voltage (pin 2,7)	V_{OH}	2.4		V	10k Ω from TTL output to +5V	Note 6
TTL output low voltage (pin 2,7)	V_{OL}		0.4	V	10k Ω from TTL output to +5V	Note 6
TTL carry high voltage (pin 11)	V_{OH}	2.4		V	5k Ω from TTL output to +5V	Note 6
TTL carry low voltage (pin 11)	V_{OL}		0.4	V	5k Ω from TTL output to +5V	Note 6
ECL carry high voltage (pin 9)	V_{OH}	-0.9	-0.7	V	V_{EE} = -5.2V (25°C)	
ECL carry low voltage (pin 9)	V_{OL}	-1.8	-1.5	V	V_{EE} = -5.2V (25°C)	
Edge speed for correct operation at maximum frequency	t_E		2.5	ns	10% to 90%	Note 7
Reset on time for correct operation	t_{ON}	100		ns		Note 7
Reset input high voltage	V_{INH}	2.4		V		Note 6
Reset input low voltage	V_{INL}		0.5	V		Note 6

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficient of V_{OH} (ECL) = +1.3mV/°C and V_{OL} = +0.5mV/°C but these are not tested.
3. The temperature coefficient of inhibited threshold voltage = +0.24mV/°C but this is not tested.
4. The test configuration for dynamic testing is shown in Fig.8.
5. Tested at 0°C and +70°C only.
6. Tested at +25°C only.
7. Guaranteed but not tested.

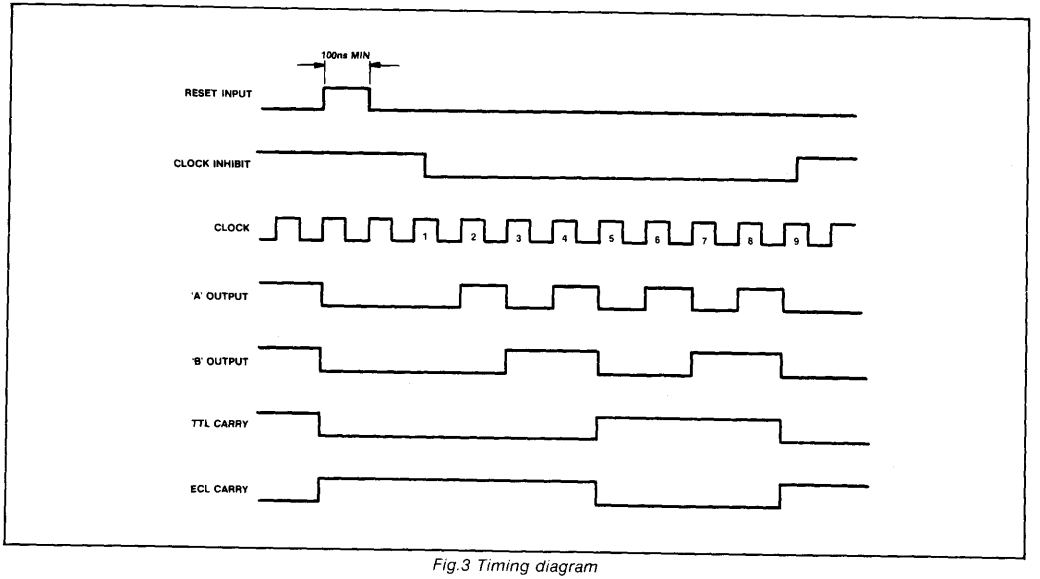
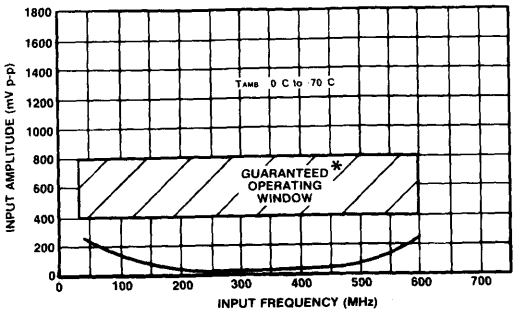


Fig.3 Timing diagram



*Tested as specified above.

Fig.4 Typical input characteristics SP8735

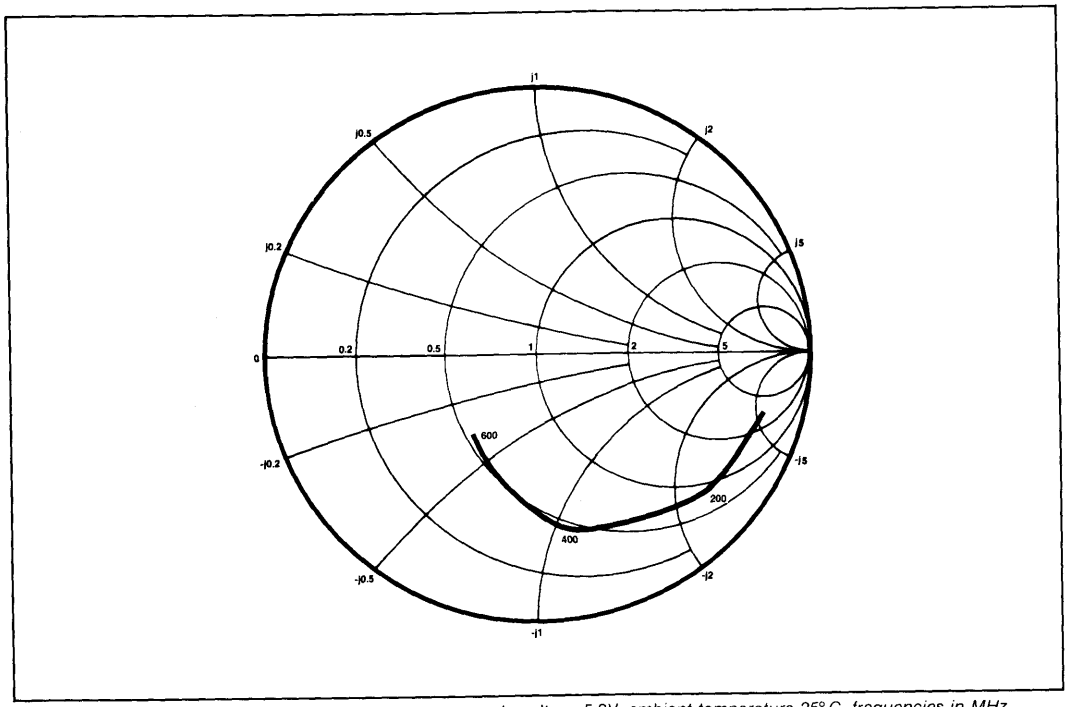


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 14) should be capacitively coupled to the signal source. The input signal path is completed by connecting a capacitor from the internal bias decoupling, pin 1 to ground.
2. In the absence of a signal the devices will self-oscillate. This can be prevented by connecting a 68k resistor between the clock input and the negative supply (pin 5).
3. The device will operate down to DC but the input slew rate must be better than 100V/μs.
4. The ECL Carry output (pin 9) is ECL II compatible but can be interfaced ECL III/10K by the inclusion of two resistors. See Fig.7.
5. The clock inhibit is compatible with ECL III/10K throughout the temperature range.
6. The 'A', 'B' and TTL Carry outputs are current sources and require the addition of 10k (pins 2 and 7) and 5k (pin 11) to +5V for TTL compatibility. See Fig. 6. This gives a fan-out = 1. The fan-out can be increased by buffering the output with a PNP emitter follower, see Fig. 9.
7. It is important to note that a positive going transition on either the clock or clock inhibit will clock the device provided of course that each input is in the low state.
8. Input impedance is a function of frequency. See Fig. 5.

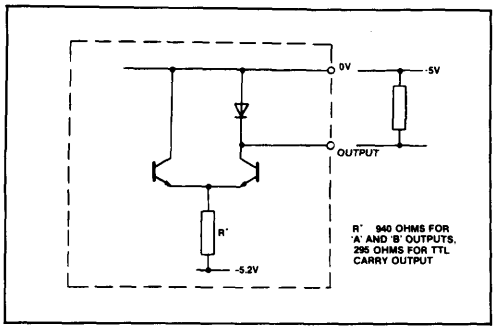


Fig.6 TTL output circuit

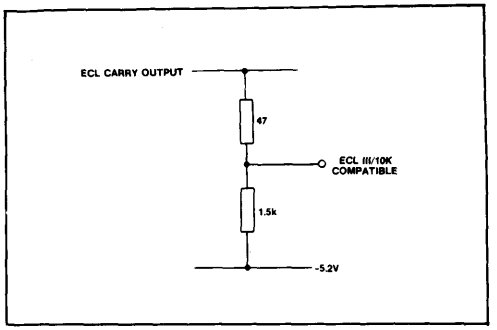


Fig.7 ECL II to ECL III/10K interface

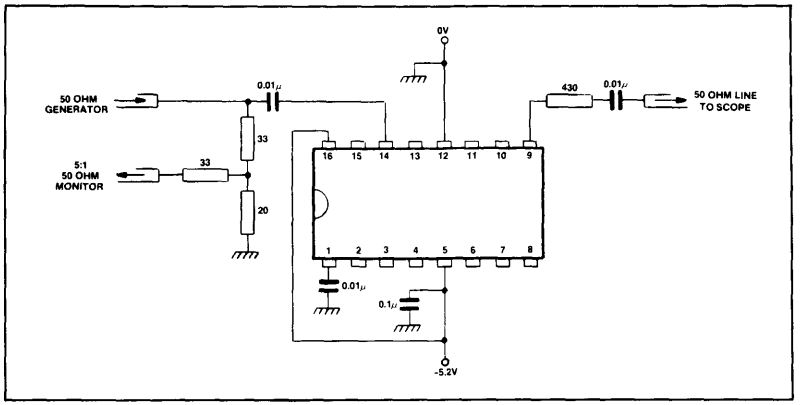


Fig.8 SP8735 high frequency test circuit

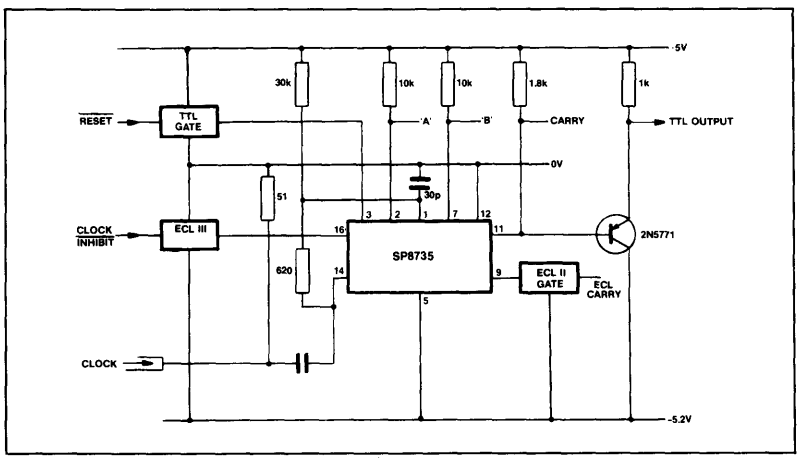


Fig.9 Typical application showing interfacing

PLESSEY
Semiconductors

SP8740A&B 300MHz ÷ 5/6
SP8741A&B 300MHz ÷ 6/7

The SP8740 and SP8741 are ECL counters with ECL 10K compatible output. The SP8740/SP8741 divide by 5 and 6 respectively when either control input is in the high state and by 6 and 7 respectively when both inputs are in the low state (or open circuit). An AC coupled input of 600mV is required.

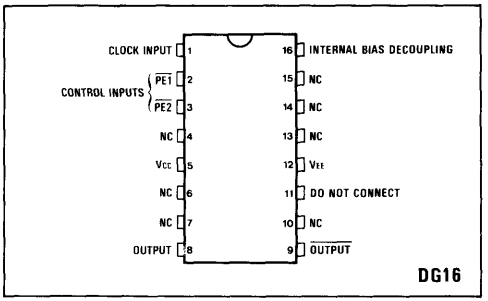


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- ECL Compatible Control Inputs
- AC Coupled Inputs (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 20mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

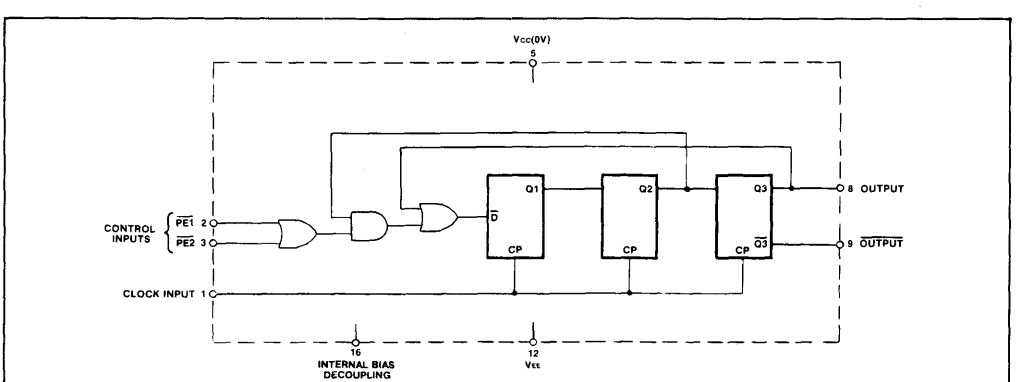


Fig.2 Functional diagram (SP8740)

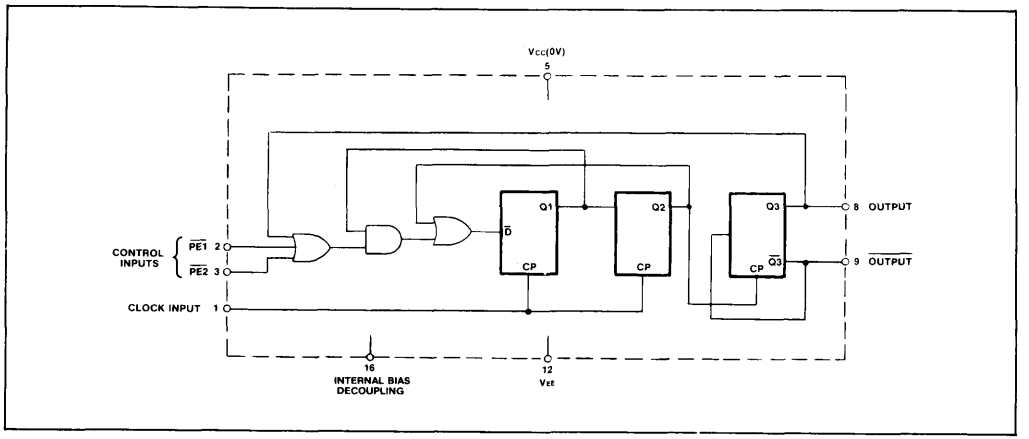


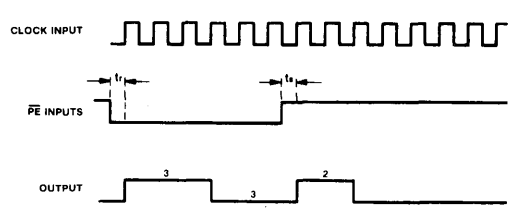
Fig.3 Functional diagram (SP8741)

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	300		MHz	Input = 400-800mV p-p	Note 3
Minimum frequency sinewave input	f_{min}		40	MHz	Input = 400-800mV p-p	Note 3
Power supply current	I_{EE}		60	mA		Note 3
ECL output high voltage	V_{OH}	-0.85	-0.7	V	V_{EE}=-5.2V(25°C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	V_{EE}=-5.2V(25°C)	
PE input high voltage	V_{INH}	-0.93		V	V_{EE}=-5.2V(25°C)	
PE input low voltage	V_{INL}		-1.62	V	V_{EE}=-5.2V(25°C)	
Clock to ECL output delay	t_p		6	ns		Note 4
Set-up time	t_s		2.5	ns		Note 4
Release time	t_r		3	ns		Note 4

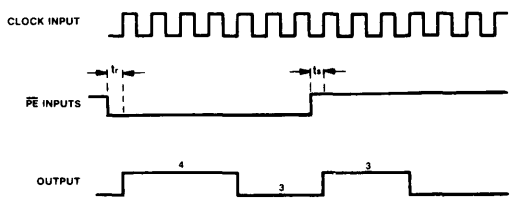
NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over the full specified supply, frequency and temperature range of both SP8740 and SP8741.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and V_{IN} = +1.22mV/°C but these are not tested.
3. SP8740/1B tested at 25°C only.
4. Guaranteed but not tested.



TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	6
H	L	5
L	H	5
H	H	5

Fig.4 Timing diagram SP8740

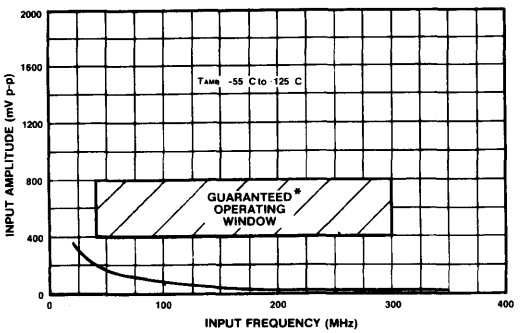


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	7
H	L	6
L	H	6
H	H	6

Fig.5 Timing diagram SP8741

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷5 or 6 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷6 or 7 mode is obtained.



* Tested as specified above.

Fig.6 Typical input characteristics SP8740/1A

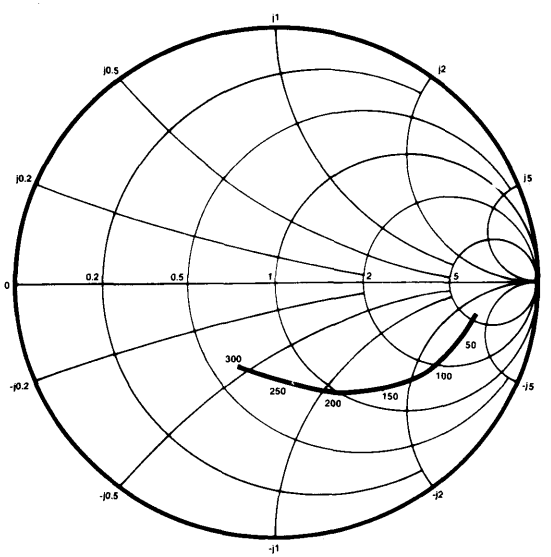


Fig.7 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/us.
4. The Q and $\overline{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 9. There is an internal circuit equivalent to a load of 2k pulldown resistor at load output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8740/1 varies as a function of frequency. See Fig. 7.
7. The SP8740 is not suitable for use in a fixed divide by 6 mode.

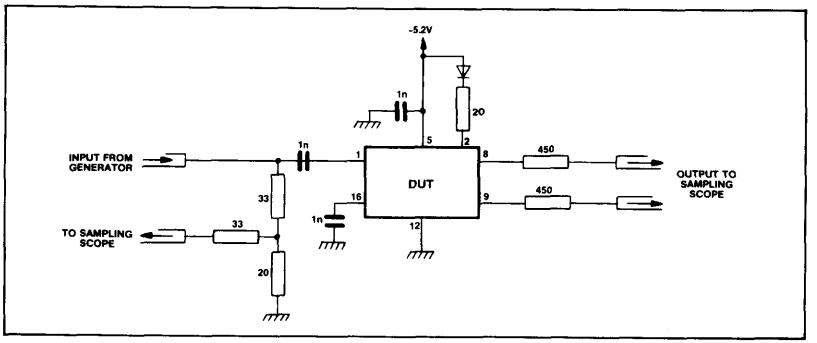


Fig.8 Test circuit

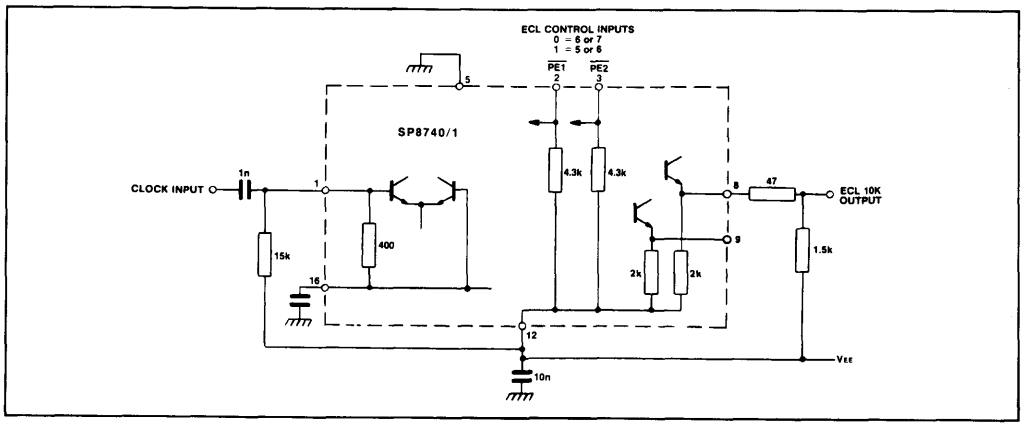


Fig.9 Typical applications circuit showing interfacing

PLESSEY
Semiconductors

SP8743A 450MHz ÷ 8/9
SP8743B 500MHz ÷ 8/9

The SP8743 is an ECL counter with ECL 10K compatible outputs. It divides by 8 when either control input is in the high state and by 9 when both inputs are low (or open circuit). An AC coupled input of 600mV p-p is required.

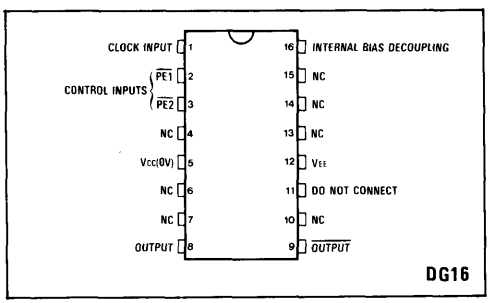


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- ECL Compatible Control Inputs
- AC Coupled Input (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 240mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: -8V
- Output Current: 20mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

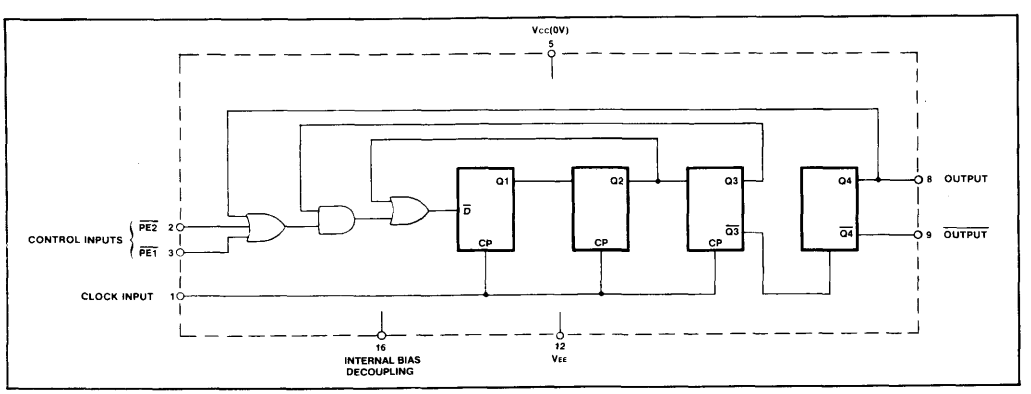


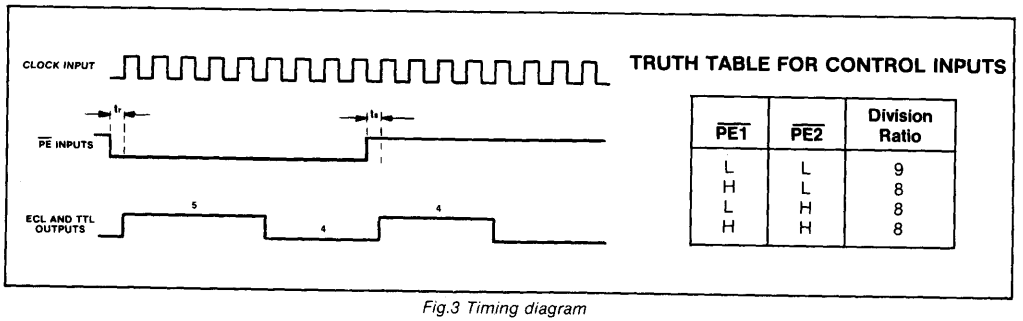
Fig.2 Function diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{EE} = -5.2 ± 0.25V V_{CC} = 0V
Temperature: A Grade T_{amb} = -55°C to +125°C
B Grade T_{amb} = -30°C to +70°C

Characteristic	Symbol	Value		Units	Grade	Conditions	Notes
		Min.	Max.				
Maximum frequency	f_{max}	450		MHz	A	Input = 400 - 800mV p-p	Note 4
sinewave input		500		MHz	B	Input = 400 - 800mV p-p	Note 4
Minimum frequency	f_{min}		40	MHz	Both	Input = 400 - 800mV p-p	Note 5
sinewave input							
Power supply current	I_{EE}		60	mA	Both	V_{EE} = -5.2V	Note 6
ECL output high voltage	V_{OH}	-0.85	-0.7	V	Both	V_{EE} = -5.2V(25° C)	
ECL output low voltage	V_{OL}	-1.8	-1.5	V	Both	V_{EE} = -5.2V(25° C)	
PE input high voltage	V_{INH}	-0.93		V	Both	V_{EE} = -5.2V(25° C)	
PE input low voltage	V_{INL}		-1.62	V	Both	V_{EE} = -5.2V(25° C)	
Clock to ECL output delay	t_p		6	ns	Both		Note 5
Set-up time	t_s	1		ns	Both		Note 5
Release time	t_r	2.5		ns	Both		Note 5

NOTES
1. Unless otherwise stated the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The temperature coefficients of V_{OH} = +1.63mV/°C, V_{OL} = +0.94mV/°C and of V_{IN} = +1.22mV/°C.
3. The test configuration for dynamic testing is shown in Fig.6.
4. Tested at low and high temperature only (not at 25°C)
5. Guaranteed but not tested.
6. Tested at 25°C only.

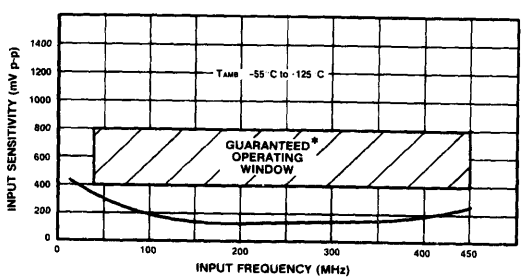


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	9
H	L	8
L	H	8
H	H	8

Fig.3 Timing diagram

NOTE:
The set-up time t_s is defined as minimum time that can elapse between L⟶H transition of control input and the next L⟶H clock pulse transition to ensure that the ÷8 mode is obtained.
The release time t_r is defined as the minimum time that can elapse between a H⟶L transition of a control input and the next L⟶H clock pulse transition to ensure that the ÷9 mode is obtained.



*Tested as specified above.

Fig.4 Typical input characteristics of SP8743A

OPERATING NOTES

1. The clock input is biased internally and is coupled to the signal source with a suitable capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting a 15k resistor from the input to V_{EE} (i.e. Pin 1 to Pin 12). This will reduce the input sensitivity by approximately 100mV.
3. The circuit will operate down to DC but slew rate must be better than 100V/μs.
4. The Q and $\overline{Q}$ outputs are compatible with ECL II but can be interfaced to ECL 10K as shown in Fig. 7. There is an internal circuit equivalent to a load of 2k pulldown resistor at each output.
5. The PE inputs are ECL III/10K compatible and include a 4.3k internal pulldown resistor. Unused inputs can therefore be left open circuit.
6. The input impedance of the SP8743 varies as a function of frequency. See Fig. 5.

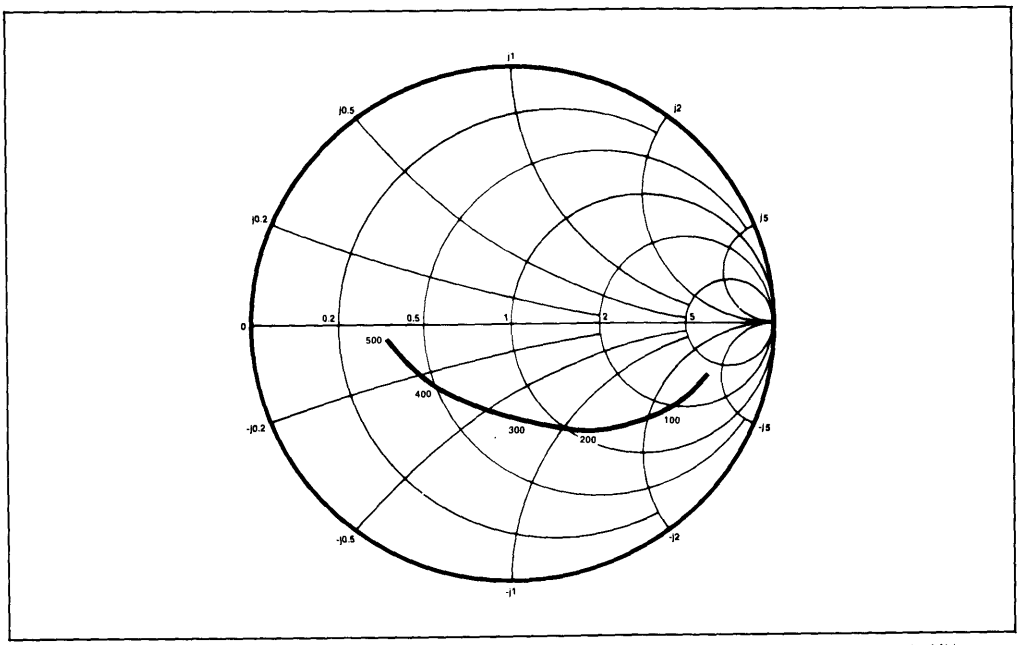


Fig.5 Typical input impedance. Test conditions: supply voltage -5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

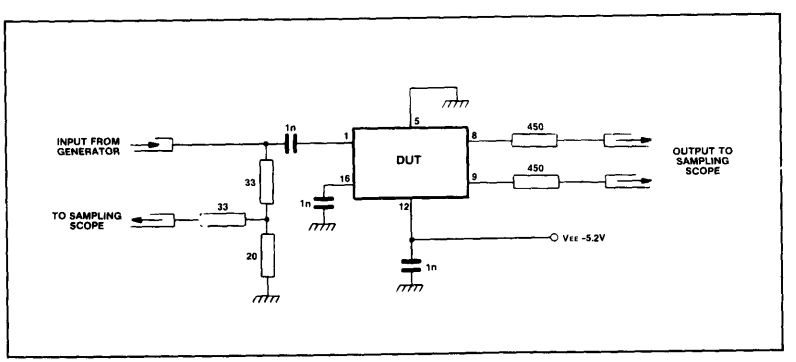


Fig.6 Test circuit

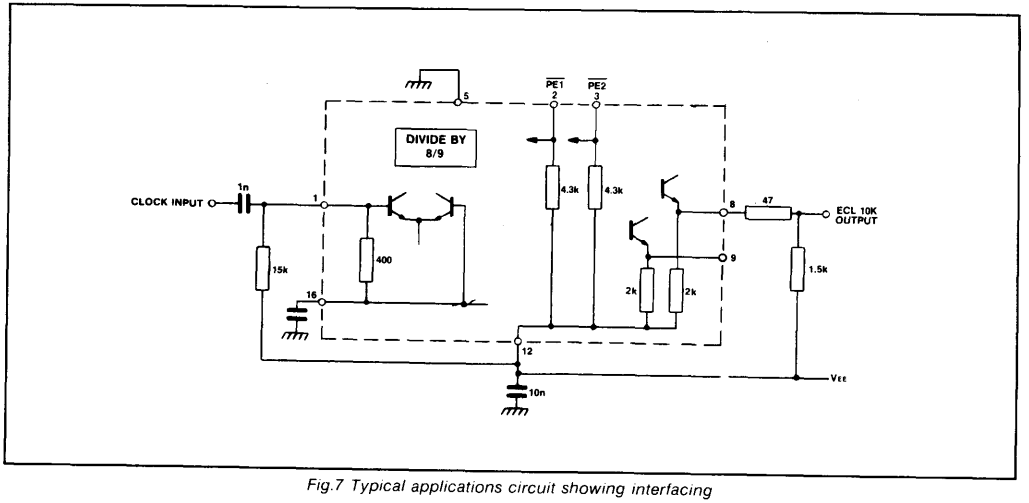


Fig.7 Typical applications circuit showing interfacing

PLESSEY
Semiconductors

SP8755A&B

1200MHz ÷ 64

The SP8755 is a divide by 64 prescaler which operates from a standard 5V TTL supply and will drive TTL directly. The SP8755A operates over the full military temperature range (-55°C to +125°C).

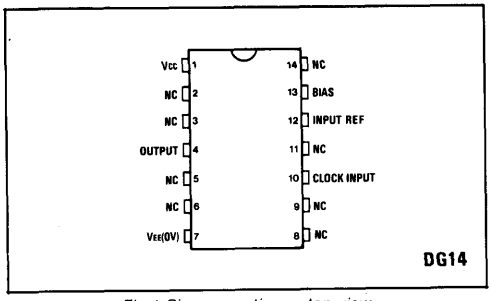


Fig.1 Pin connections - top view

FEATURES

- TTL Compatible Output
- AC Coupled Input (Internal Bias)

QUICK REFERENCE DATA

- Supply Voltage: 5V
- Power Consumption: 270mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Output Current: ±30mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Input Voltage: 2.5V p-p

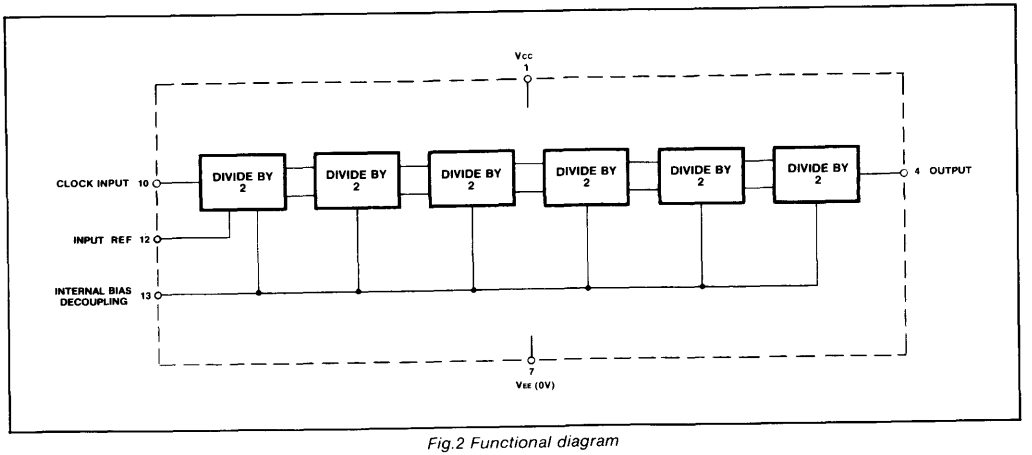


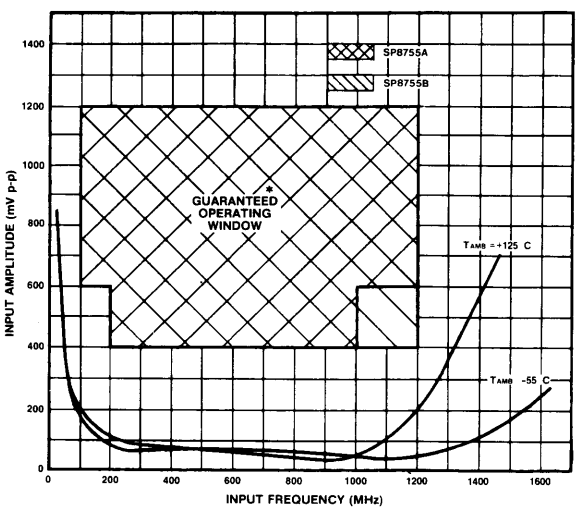
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.0 ± 0.25V V_{EE} = 0V
Temperature: A grade T_{amb} = -55°C to +125°C
B grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value		Units	Grade	Conditions
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	1.2		GHz	SP8755A	Input = 600-1200mV p-p
		1.2		GHz	SP8755B	Input = 400-1200mV p-p
Minimum frequency sinewave input	f_{min}		100	MHz	Both	Input = 600-1200mV p-p
Power supply current	I_{EE}		75	mA	Both	
Output high voltage	V_{OH}	2.5		V	Both	
Output low voltage	V_{OL}		0.45	V	Both	Sink current = 5mA

NOTES
1. Unless otherwise stated,the electrical characteristics shown above are guaranteed over specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.5.
3. Above characteristics are not tested at 25°C (tested at low and high temperature only).



*Tested as specified above.

Fig.3 Typical input characteristics SP8755A B

OPERATING NOTES

1. The clock input is biased internally and is connected to the signal source via a capacitor. The input signal path is completed by an input reference decoupling capacitor which is connected to earth.
2. If no signal is present the device will self-oscillate. If this is undesirable it may be prevented by connecting an 18k resistor between input and V_{EE} (i.e. Pin 10 to Pin 7). This will reduce sensitivity by approximately 100mV.
3. The device will operate down to DC but input slew rate must be better than 100V/µs.
4. The output stage is a standard totem pole TTL and can therefore be interfaced directly to TTL.

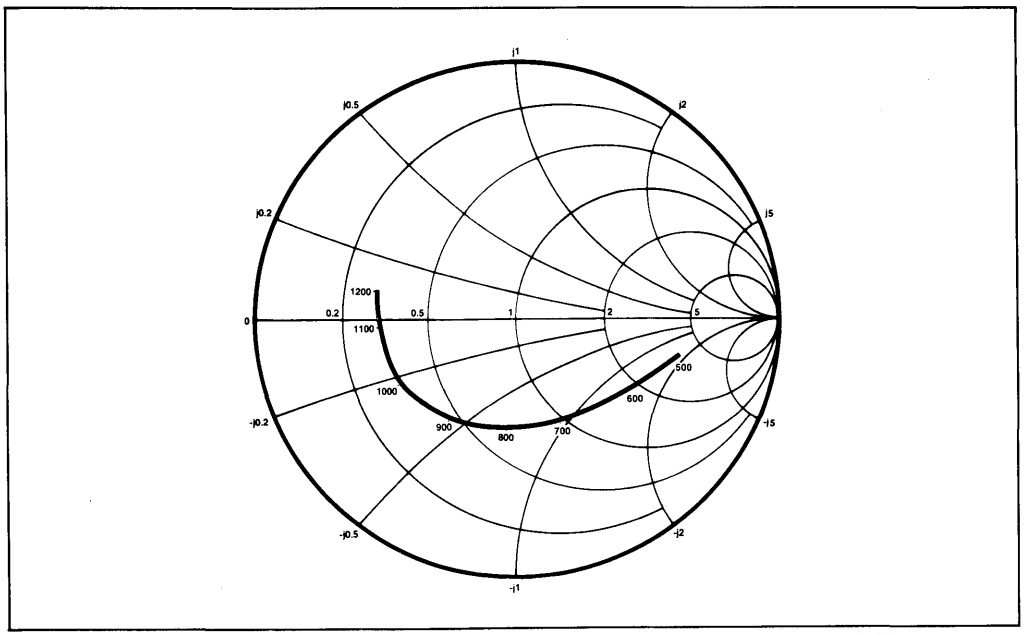


Fig.4 Typical input impedance. Test conditions: supply voltage 5V, ambient temperature 25°C. Frequencies in MHz, impedances normalised to 50 ohms.

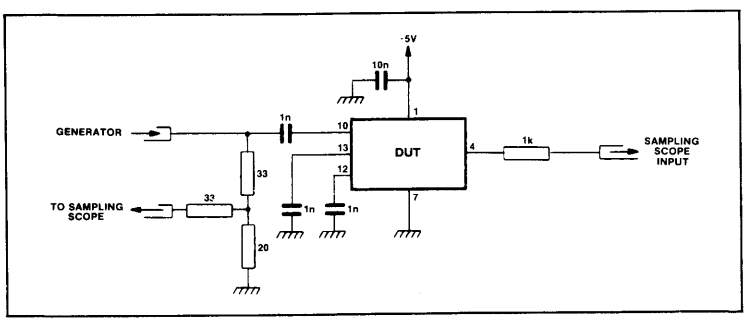


Fig.5 Test circuit

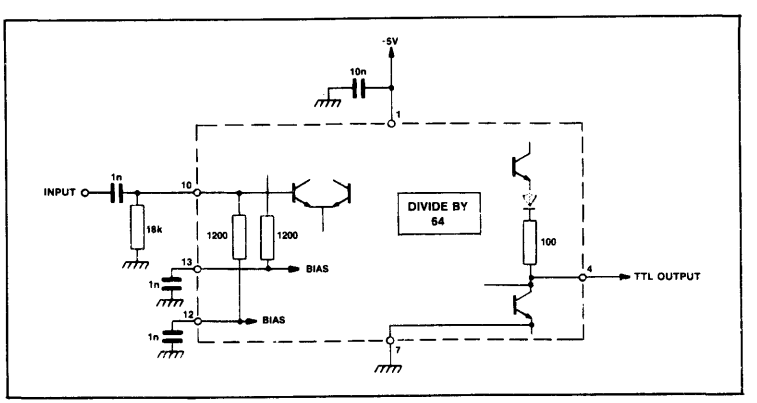


Fig.6 Typical applications circuit showing interfacing

PLESSEY
Semiconductors

SP8785A&B 1000MHz ÷ 20/22
SP8786A&B 1300MHz ÷ 20/22

The SP8785 and SP8786 are high speed 2 modulus counters for use up to 1.0 and 1.3GHz respectively. They feature ECL compatible control inputs and outputs and are available in either the -30°C to +70°C (B Grade) or -55°C to +125°C (A Grade) temperature ranges.

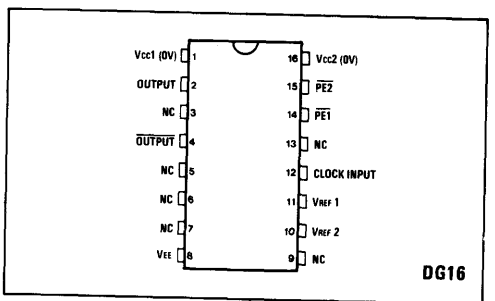


Fig.1 Pin connections - top view

FEATURES

- ECL Compatible Outputs
- AC Coupled Input
- Control Inputs ECL Compatible

QUICK REFERENCE DATA

- Supply Voltage: -5.2V
- Power Consumption: 450mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Output Current: 20mA
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

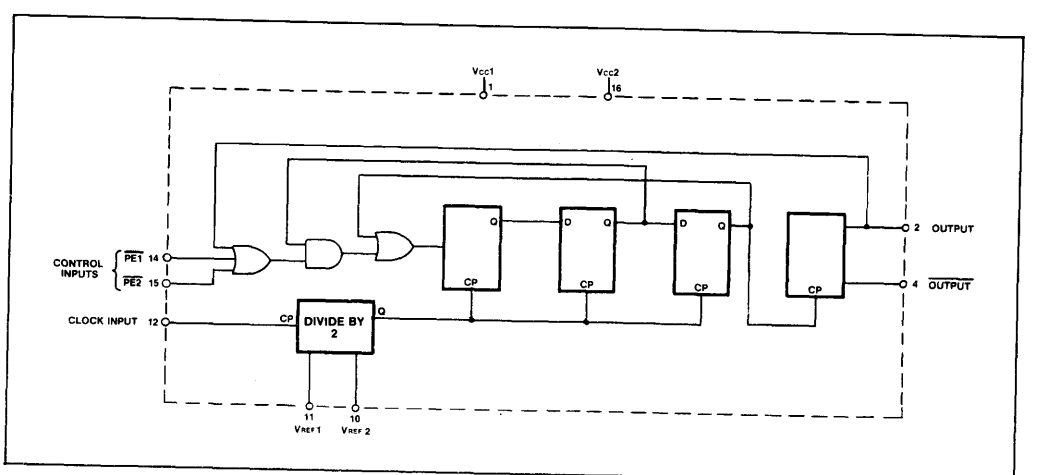


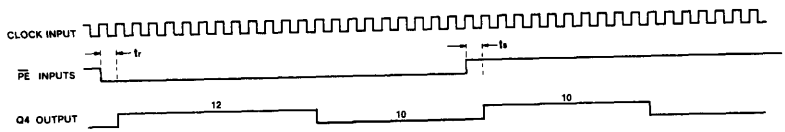
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 0V V_{EE} = -5.2V ± 0.25V
Temperature: A grade T_{case} = -55°C to +125°C (case temperature)
B grade T_{amb} = -30°C to +70°C

Characteristics	Symbol	Value Min.	Value Max.	Units	Grade	Conditions	Notes
Maximum toggle frequency sinewave input	f_{max}	1.0		GHz	SP8785	Input = 400-1200mV p-p	Note 4
		1.3		GHz	SP8786	Input = 600-1200mV p-p	Note 4
		1.3		GHz	SP8786	Input = 400-1200mV p-p	Note 4
Minimum toggle frequency sinewave input	f_{min}		150	MHz	All	Input = 400-1200mV p-p	Note 5
Current consumption	I_{EE}		115	mA	All	V_{EE} = -5.2V outputs unloaded	Note 6
Output low voltage	V_{OL}	-1.85	-1.62	V	All	V_{EE} = -5.2V output load = 430Ω	
Output high voltage	V_{OH}	-0.93	-0.78	V	All	V_{EE}=-5.2V(25°C) output load = 430Ω	
Minimum output swing	V_{OUT}	500		mV	All	V_{EE}=-5.2V(25°C) output load = 430Ω	Note 4
Clock to output delay	t_p		4	ns	All	V_{EE} = -5.2V	Note 5
Set up time	t_s	1		ns	All	V_{EE} = -5.2V	Note 5
Release time	t_r	1		ns	All	V_{EE} = -5.2V	Note 5
PE input high voltage	V_{INH}	-0.93		V	All	V_{EE}=-5.2V(25°C)	
PE input low voltage	V_{INL}		-1.62	V	All	V_{EE}=-5.2V(25°C)	

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over specified supply, frequency and temperature range.
2. The A grade devices must be used with a heat sink to maintain chip temperature below +175°C when operating at an ambient of +125°C.
3. The temperature coefficient of V_{INL} & V_{INH} = +0.8mV/°C, of V_{OH} = +1.2mV/°C but these are not tested.
4. Tested at low and high temperatures only.
5. Guaranteed but not tested.
6. Tested at 25°C only.

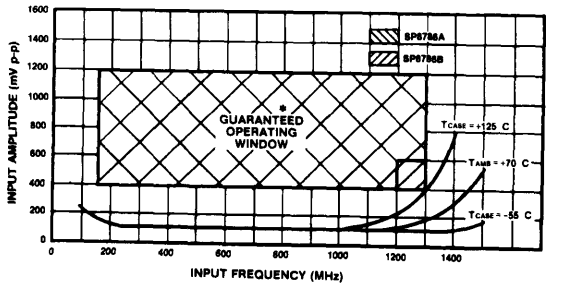


TRUTH TABLE FOR CONTROL INPUTS

$\overline{PE1}$	$\overline{PE2}$	Division Ratio
L	L	22
H	L	20
H	H	20
H	H	20

Fig.3 Timing diagram

NOTES
The set up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure ÷20 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷22 mode is selected.



*Tested as specified above.

Fig.4 Typical characteristics SP8786

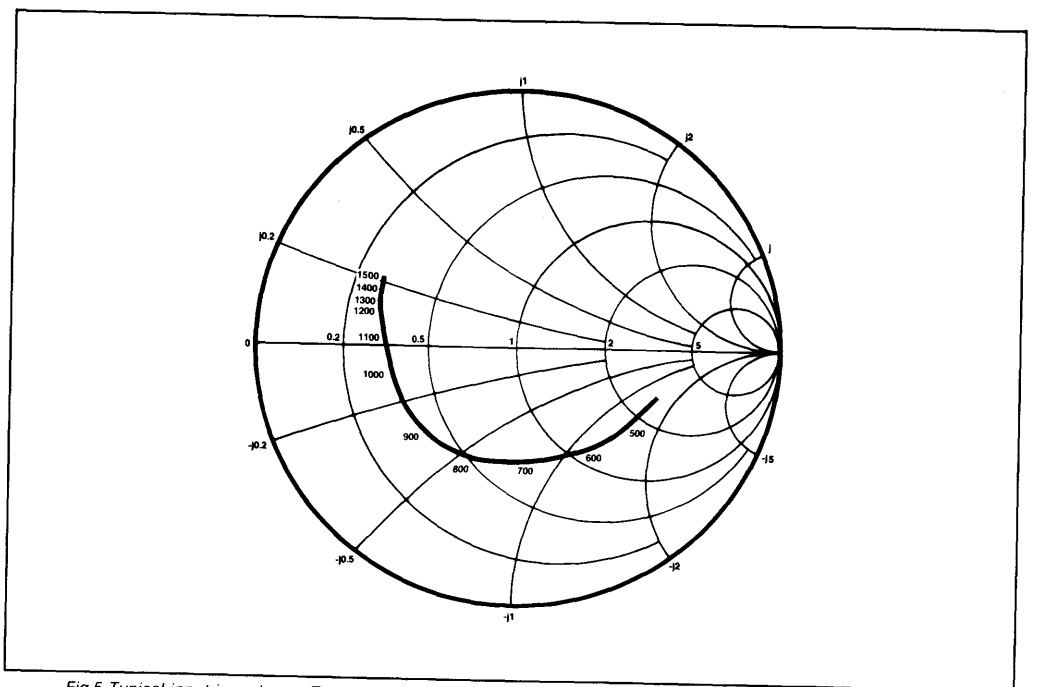


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

OPERATING NOTES

1. The clock input (pin 12) should be capacitively coupled to the signal source. The input signal path is completed by connecting a decoupling capacitor from $V_{REF}1$ (pin 11) to ground. $V_{REF}2$ (pin 10) should also be decoupled with a suitable capacitor, see Figs. 6 and 7.
2. If no signal is present the circuit device will self-oscillate. If this is undesirable it may be prevented by connecting a 10k resistor from the input to V_{EE} (i.e. pin 12 to pin 8).
3. The input can be operated at very low frequencies but slew rate must be better than 200V/µs.
4. The emitter follower outputs require a 430Ω pull-down resistor and are compatible with ECL III/10K. An equal load on an unused output will reduce distortion.
5. The PE inputs are ECL III/10K compatible and include a 4.3k pull-down resistor. Unused inputs can therefore be left open.
6. The input impedance of the SP8785/6 is a function of frequency, see Fig. 5. These impedance variations may give the effect of large variations in sensitivity because of the loading of the source by the device. For best results impedance matching should be used.
7. Note that all components should be suitable for the frequency in use.

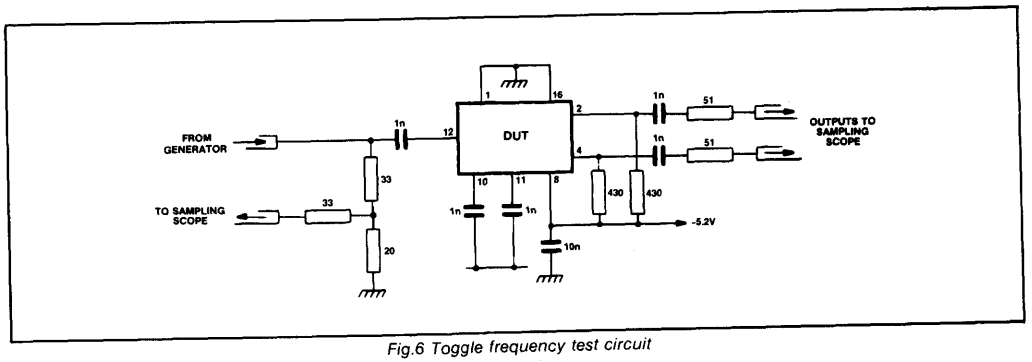


Fig.6 Toggle frequency test circuit

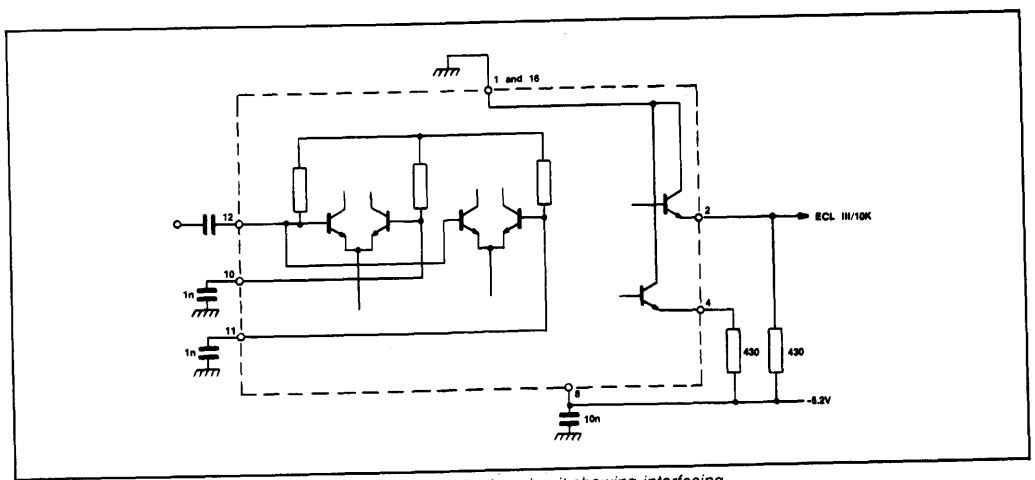


Fig.7 Typical application circuit showing interfacing

PLESSEY
Semiconductors

SP8790A&B

60MHz ÷ 4 (2-MODULUS EXTENDER)

The SP8790 is a divide-by-four counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratio. Suitable for low power frequency synthesis interfacing to CMOS or TTL.

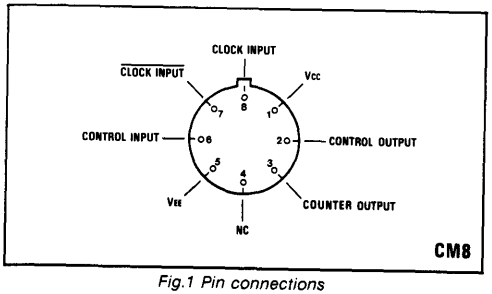


Fig.1 Pin connections

FEATURES

- Very Low Power
- Control Input and Counter Output will Interface Directly to TTL or CMOS
- Interfaces to SP8000 Programmable 2 Modulus Counters

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 40mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Open Collector Output: 12V
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p
- Output Sink Current: 10mA

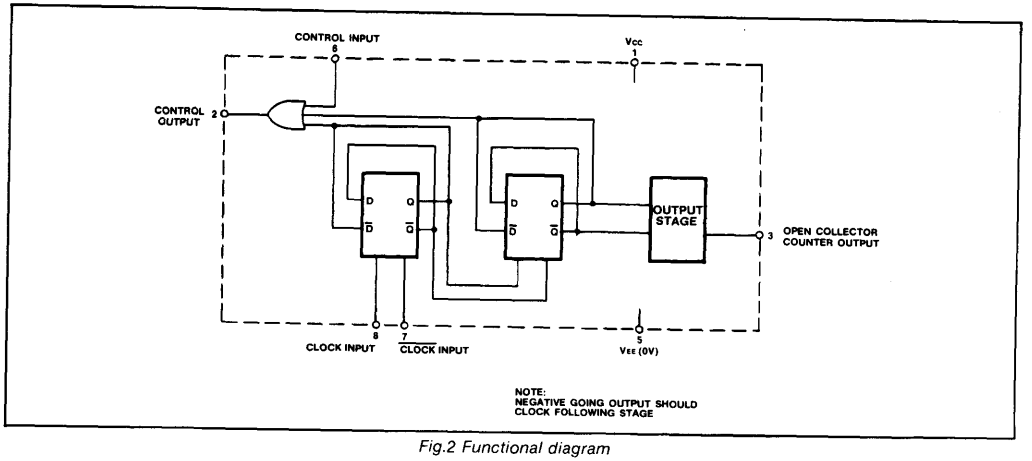


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5V ± 0.25V V_{EE} 0V
Temperature: A grade: -55 C to +125 C
B grade: -30 C to +70 C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	60		MHz	Tested as a controller. See Fig.4	Note 3
Power supply current	I_{EE}		11	mA		Note 3
Control input high voltage	V_{INH}	3.5	10	V		Note 3
Control input low voltage	V_{INL}	0	1.5	V		Note 3
Output high voltage (pin 3)	V_{OH}	9		V	Pin 3 via 1.6k to +10V	Note 3
Output low voltage (pin 3)	V_{OL}		0.4	V	Pin 3 via 1.6k to +10V	Note 3
Output high voltage (pin 2)	V_{OH}	4.27	4.5	V	V_{CC} = 5.2V (25° C)	
Output low voltage (pin 2)	V_{OL}	3.28	3.7	V	V_{CC} = 5.2V (25° C)	
Clock to counter output -ve going delay	t_{pHL}		25	ns		Note 4
Clock to counter output +ve going delay	t_{pLH}		40	ns		Note 4
Clock to control output -ve going delay	t_{pLH}		15	ns	10kΩ pull-down on control O/P	Note 4
Clock to control output +ve going delay	t_{pHL}		26	ns	10kΩ pull-down on control O/P	Note 4
Control input to control output -ve going delay	t_{pLH}		12	ns	10kΩ pull-down on control O/P	Note 4
Control input to control output +ve going delay	t_{pHL}		16	ns	10kΩ pull-down on on control O/P	Note 4

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.4.
3. Tested at low and high temperatures only.
4. Guaranteed but not tested.

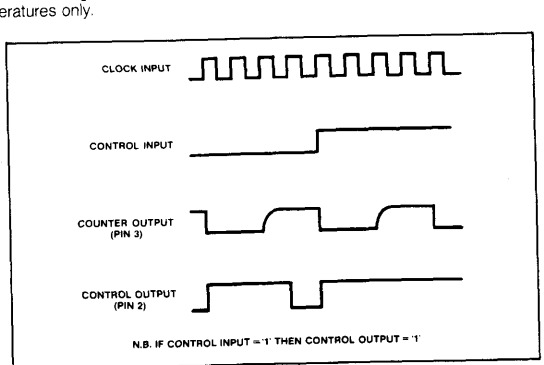


Fig.3 Timing diagram

OPERATING NOTES

1. The device will normally be driven by capacitively coupling the inputs to outputs of a 2-modulus divider. See Figs. 4 and 5. The maximum frequency of the device when used as a controller is limited by the internal delays and will not operate above 60MHz. When used as a prescaler the device will operate in excess of 80MHz, the maximum frequency being limited by saturation of the counter output stage.
2. The device is normally driven from very fast edges of a 2-modulus divider and therefore there is no input slew rate problem.
3. The control input is TTL/CMOS compatible.
4. The counter output (pin 3) interfaces into CMOS/TTL by the addition of a pull-up resistor. For interconnecting to CMOS the output can be connected via a pull-up resistor to supply which should not exceed 12V.
5. When used as a controller the circuit will self-oscillate. This can be prevented by using one of the arrangements as shown in Fig. 5.
6. The control output, which includes an internal 16k pull-down resistor is ECL compatible and interfaced directly into, for example, SP8695. See Fig. 5.
7. The propagation delays stated are with a 10k pull-down resistor which is input pull-down of the SP8695. For interfacing into the SP8643/47 series which have 4.3k pull-downs, the propagation delays will be reduced.

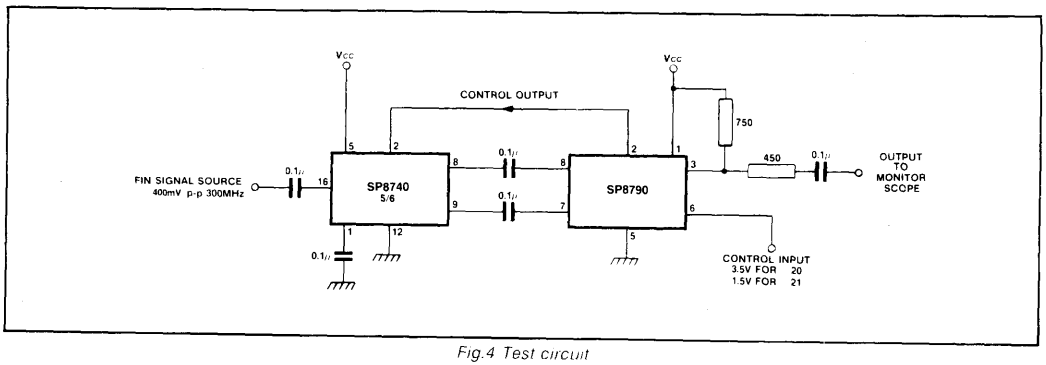


Fig.4 Test circuit

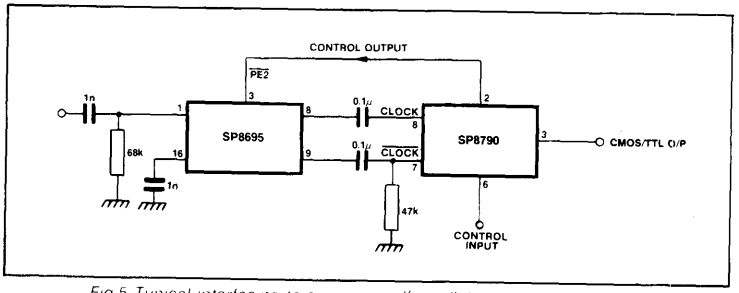


Fig.5 Typical interfacing to suppress self oscillation with no input signal

PLESSEY
Semiconductors

SP8792 225MHz ÷ 80/81
SP8793 225MHz ÷ 40/41

WITH ON-CHIP VOLTAGE REGULATOR

The SP8792 and SP8793 are low power programmable ÷80/81 and ÷40/41 counters, temperature range: -40°C to +85°C. They divide by 80(40) when control input is in the high state and by 81(41) when in the low state. An internal voltage regulator allows operation from a wide range of supply voltages.

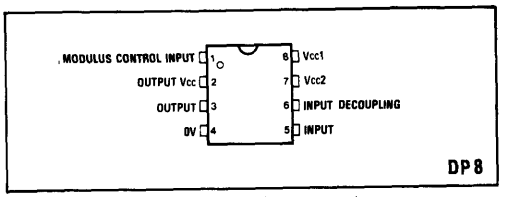


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input
- Operation up to 9.5V using Internal Regulator

QUICK REFERENCE DATA

- Supply Voltage: +5.2V or 6.8V to 9.5V
- Power Consumption: 26mW

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 6.0V pins 7 & 8 tied
- Supply Voltage: 13.5V pin 8, pin 7 decoupled
- Storage Temperature Range: -40°C to +85°C
- Max. Junction Temperature: +175°C
- Max. Clock Input Voltage: 2.5V p-p

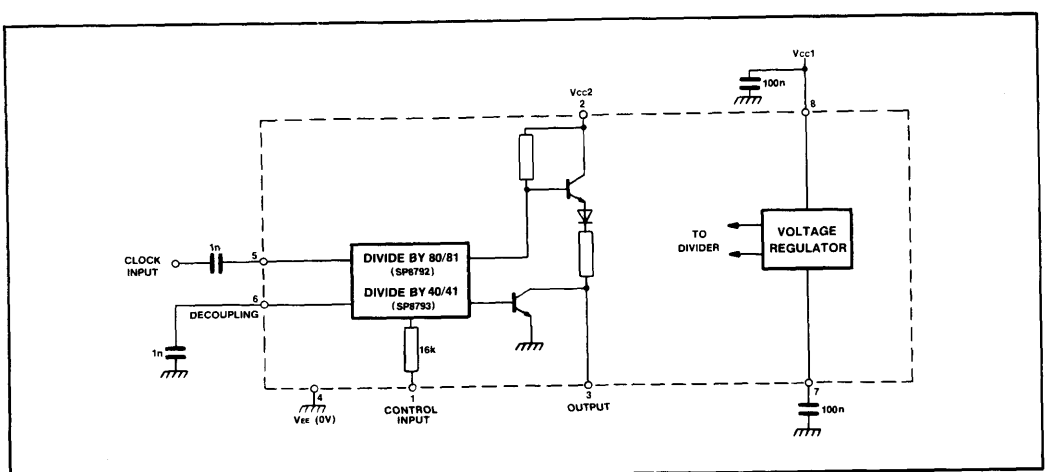


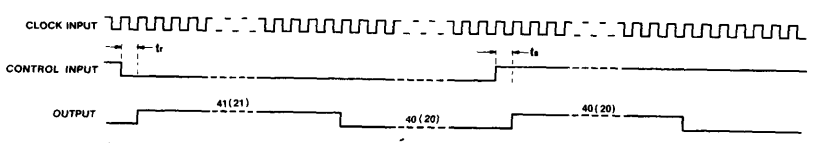
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ± 0.25V or 6.8-9.5V (See Operating Note 6) V_{EE} 0V
Temperature: T_{amb} -40°C to +85°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	225		MHz	Input = 200-800mV p-p	Note 4
Minimum frequency (sinewave input)	f_{min}		20	MHz	Input = 400mV p-p	Note 4
Power supply current	I_{EE}		7	mA		Note 4
Control input high voltage	V_{INH}	4		V		Note 4
Control input low voltage	V_{INL}		2	V		Note 4
Output high voltage	V_{OH}	2.4		V	Pins 2,7 and 8 linked V_{CC} = 4.95V I_{OH} = 100µA	Note 4
Output low voltage	V_{OL}		0.5	V	Pin 2 open or linked to 8 and 7 I_{OL} = 1.6mA	Note 4
Set up time	t_s	14		ns	25°C	Note 3
Release time	t_r	20		ns	25°C	Note 3
Clock to output propagation time	t_p		45	ns	25°C	Note 3

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

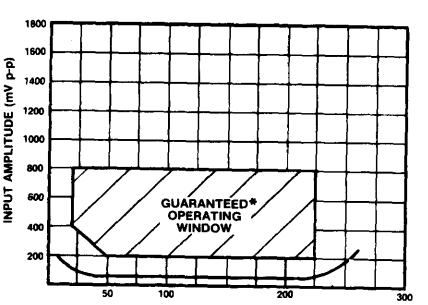


TRUTH TABLE FOR CONTROL INPUTS

Control Inputs	Division Ratio	
	SP8792	SP8793
0	81	41
1	80	40

Fig.3 Timing diagram SP8792/3

NOTES
The set-up time t_s is defined as minimum time that can elapse between L→H transition of control input and the next L→H clock pulse transition to ensure ÷80 or 40 mode is selected.
The release time t_r is defined as minimum time that can elapse between H→L transition of the control input and the next L→H clock pulse transition to ensure the ÷81 or 41 mode is selected.



* Tested as specified above.

Fig.4 Input sensitivity SP8792/SP8793

OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, pin 6 to ground.
2. The output stage which is normally open collector (pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k or greater resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then pin 2, 7, and 8 should be connected together to give a fan-out = 1. Alternatively, the open collector output may be used with a pull-up resistor.
3. The circuit will operate down to DC but a slew rate of better than 20V/μs is required.
4. The mark space ratio of the output is 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig. 5.
6. If no signal is present the circuit will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The supply voltage regulator which allows the SP8792/3 to be used at supply voltages up to 9.5V is NOT available for use in the A Grade device: the SP8792A and SP8793A are ONLY available for operation from 5.2V supply, and therefore pins 7 and 8 should always be externally connected together.

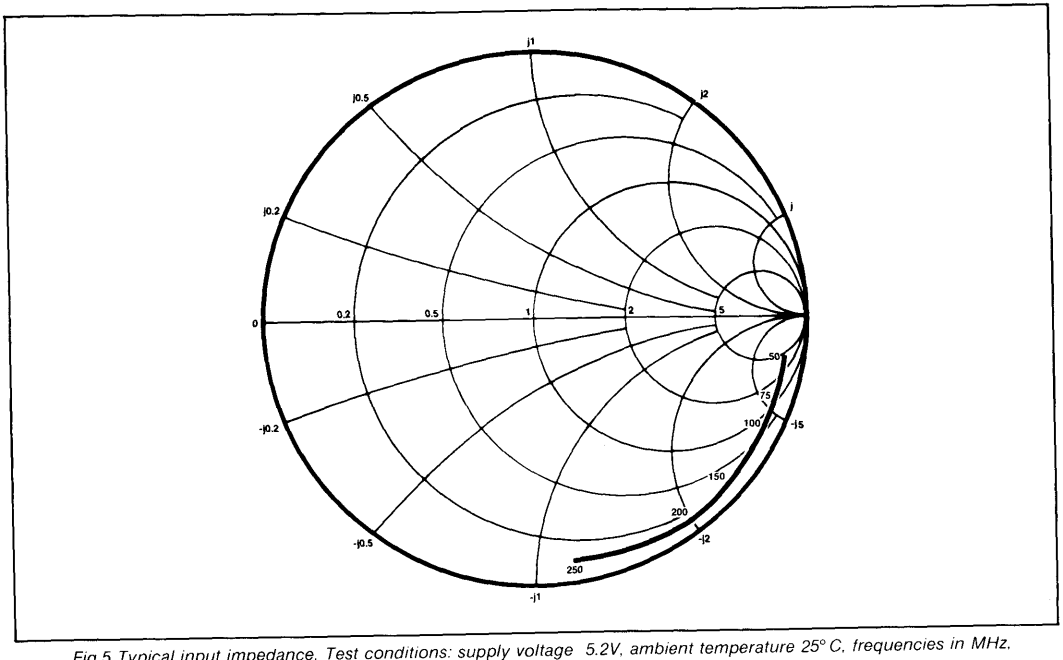


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

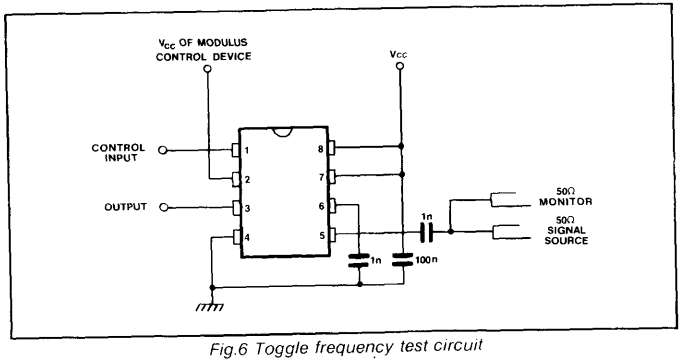


Fig.6 Toggle frequency test circuit

PLESSEY
Semiconductors

SP8792A 200MHz ÷ 80/81
SP8793A 200MHz ÷ 40/41

The SP8792A and SP8793A are low power programmable +80/81 and +40/41 counters which operate over the full Military temperature range. They divide by 80(40) when the control input is in the high state and by 81(41) when in the low state.

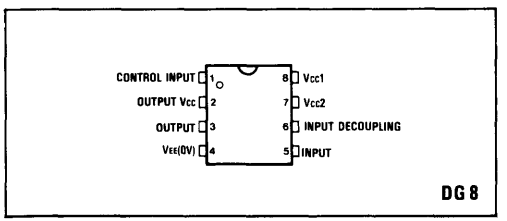


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Output CMOS/TTL Compatible
- AC Coupled Input

QUICK REFERENCE DATA

- Supply Voltage: +5.2V
- Power Consumption: 26mW typical
- Temperature Range: -55°C to +125°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 6V pins 7 & 8 linked
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Clock I/P Voltage: 2.5V p-p

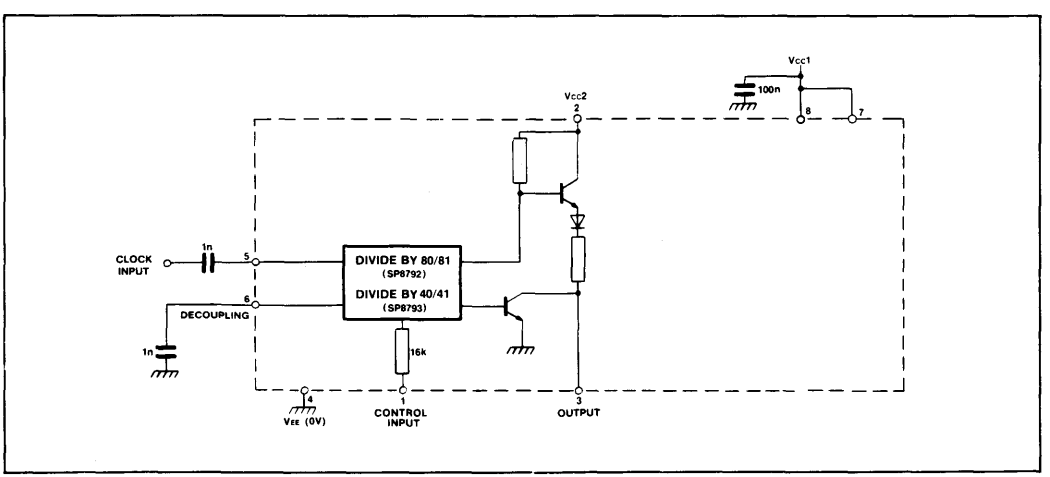


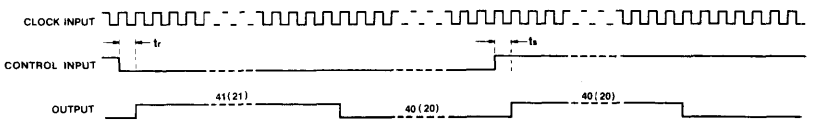
Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5.2V ± 0.25V V_{EE} = 0V
Temperature: T_{amb} = -40°C to +85°C

Characteristic	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency (sinewave input)	f_{max}	200		MHz	Input =200 - 400mV p-p	
		150		MHz	Input =200 - 800mV p-p	Note 3
Minimum frequency (sinewave input)	f_{min}		20	MHz	Input =400mV p-p	
Power supply current	I_{EE}		7	mA		Note 4
Control input high voltage	V_{INH}	4		V		Note 4
Control input low voltage	V_{INL}		2	V		Note 4
Output high voltage	V_{OH}	2.4		V	Pins 2,7 and 8 linked V_{CC}= 4.95V I_{OH}= -100μA	Note 4
Output low voltage	V_{OL}		0.5	V	Pin 2 linked to 8 and 7 I_{OL} = 1.6mA	Note 4
Set-up time	t_s	14		ns	25°C	Note 3
Release time	t_r	20		ns	25°C	Note 3
Clock to output propagation time	t_p		45	ns	25°C	Note 3

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full specified supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.6.
3. Guaranteed but not tested.
4. Tested at 25°C only.

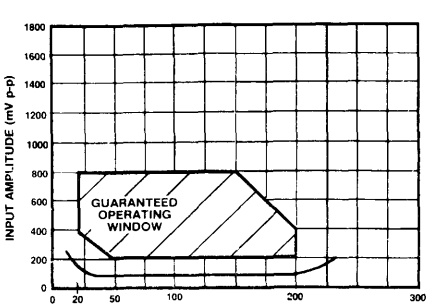


TRUTH TABLE FOR CONTROL INPUTS

Control Inputs	Division Ratio	
	SP8792A	SP8793A
0	81	41
1	80	40

Fig.3 Timing diagram (SP8792/3A)

NOTE
The set-up time t_s is defined as the minimum time t_s that can elapse between a L→H transition of the control input and the next L→H clock pulse transition to ensure that the ÷80(40) mode is selected.
The release time t_r is defined as the minimum time that can elapse between a H→L transition of the control input and the next L→H clock pulse transition to ensure that the ÷81(41) mode is selected.



*Tested as specified above.

Fig.4 Input sensitivity (SP8792/3A)

OPERATING NOTES

1. The clock input (pin 5) should be capacitively coupled to the signal source. The input signal path is completed by coupling a capacitor from the internal bias decoupling, pin 6 to ground.
2. The output stage which is normally open collector (pin 2 open circuit) can be interfaced to CMOS. The open collector can be returned to a +10V line via a 5k or greater resistor but the output sink current should not exceed 2mA. If interfacing to TTL is required then pin 2, 7, and 8 should be connected together to give a fan-out = 1. Alternatively, the open collector output may be used with a pull-up resistor.
3. The circuit will operate down to DC but a slew rate of better than 20V/µs is required.
4. The mark space ratio of the output is 1.2:1 at 200MHz.
5. Input impedance is a function of frequency. See Fig. 5.
6. If no signal is present the circuit will self-oscillate. If this is undesirable it may be prevented by connecting a 150k between unused input and ground. This reduces the input sensitivity by typically 50-100mV p-p.
7. The supply voltage regulator which allows the SP8792/3 to be used at supply voltages up to 15V is NOT available for use in the A Grade device: the SP8792A and SP8793A are ONLY available for operation from 5.2V supply, and therefore pins 7 and 8 should always be externally connected together.

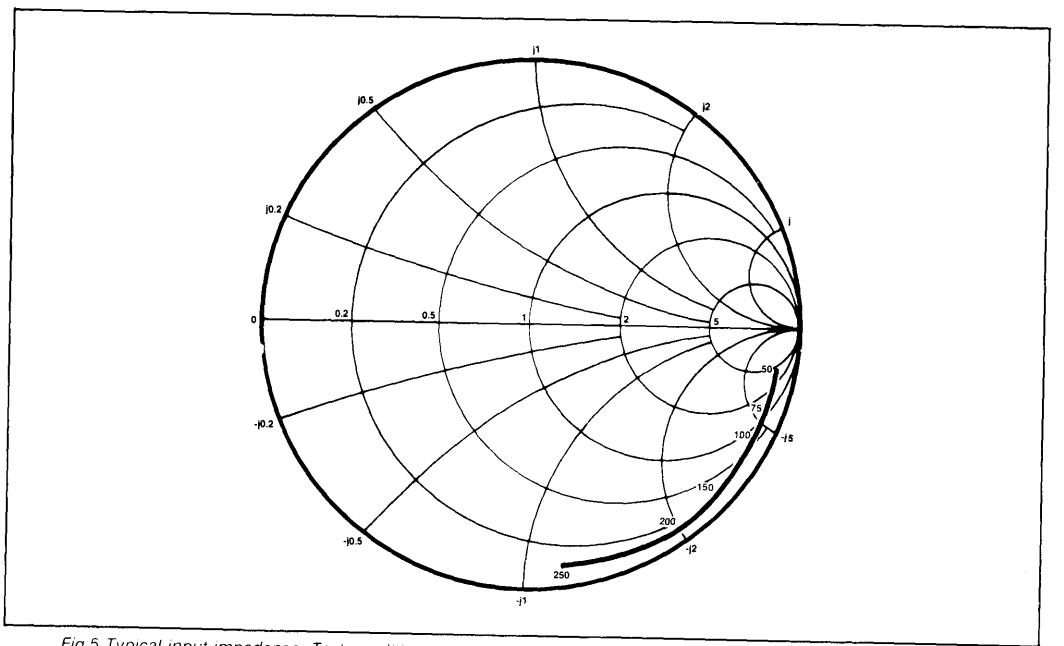


Fig.5 Typical input impedance. Test conditions: supply voltage 5.2V, ambient temperature 25° C, frequencies in MHz, impedances normalised to 50 ohms.

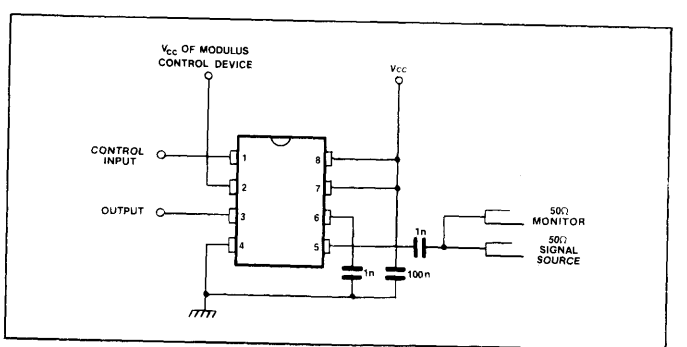


Fig.6 Toggle frequency test circuit

PLESSEY
Semiconductors

SP8794A&B

60MHz ÷ 8 (2-MODULUS EXTENDER)

The SP8794 is a divide-by-eight counter designed for use with 2-modulus counters. It increases the minimum division ratio of the 2-modulus counter while retaining the same difference in division ratio. Suitable for low power frequency synthesis interfacing to CMOS or TTL.

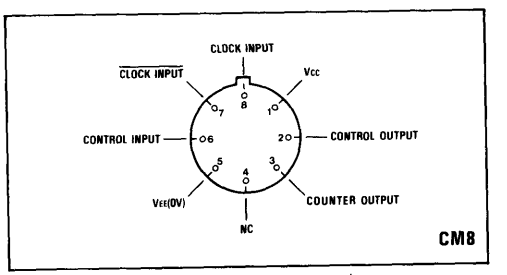


Fig.1 Pin connections - top view

FEATURES

- Very Low Power
- Control Input and Counter Output will Interface Directly to TTL or CMOS
- Interfaces to SP8000 Programmable 2-Modulus Counters

QUICK REFERENCE DATA

- Supply Voltage: 5.0V
- Power Consumption: 40mW
- Temperature Range:
  - A Grade: -55°C to +125°C
  - B Grade: -30°C to +70°C

ABSOLUTE MAXIMUM RATINGS

- Supply Voltage: 8V
- Open Collector Output: 12V
- Storage Temperature Range: -55°C to +150°C
- Max. Junction Temperature: +175°C
- Max. Input Voltage: 2.5V p-p
- Output Sink Current: 10mA

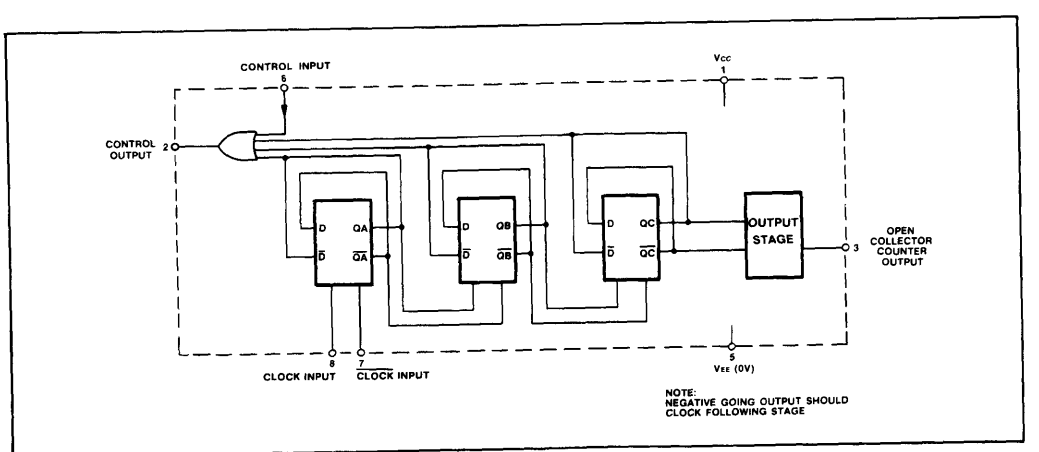


Fig.2 Functional diagram

ELECTRICAL CHARACTERISTICS

Supply Voltage: V_{CC} = 5V ± 0.25V V_{EE} = 0V
Temperature: A grade: -55°C to +125°C
B grade: -30°C to +70°C

Characteristics	Symbol	Value		Units	Conditions	Notes
		Min.	Max.			
Maximum frequency sinewave input	f_{max}	60		MHz	Tested as a controller. See Fig. 4	Note 3
Power supply current	I_{EE}		11	mA		Note 3
Control input high voltage	V_{INH}	3.5	10	V		Note 3
Control input low voltage	V_{INL}	0	1.5	V		Note 3
Output high voltage (pin 3)	V_{OH}	9		V	Pin 3 via 1.6k to +10V	Note 3
Output low voltage (pin 3)	V_{OL}		0.4	V	Pin 3 via 1.6k to +10V	Note 3
Output high voltage (pin 2)	V_{OH}	4.27	4.5	V	Vcc = 5.2V(25° C)	
Output low voltage (pin 2)	V_{OL}	3.28	3.7	V	Vcc = 5.2V(25° C)	
Clock to counter output -ve going delay	t_{pHL}		27	ns		Note 4
Clock to counter output +ve going delay	t_{pLH}		48	ns		Note 4
Clock to control output -ve going delay	t_{pLH}		15	ns	10k pull-down on control O/P	Note 4
Clock to control output +ve going delay	t_{pHL}		26	ns	10k pull-down on control O/P	Note 4
Control input to control output -ve going delay	t_{pLH}		12	ns	10k pull-down on control O/P	Note 4
Control input to control output +ve going delay	t_{pHL}		16	ns	10k pull-down on on control O/P	Note 4

NOTES
1. Unless otherwise stated the electrical characteristics are guaranteed over full supply, frequency and temperature range.
2. The test configuration for dynamic testing is shown in Fig.4.
3. Tested at low and high temperatures only.
4. Guaranteed but not tested.

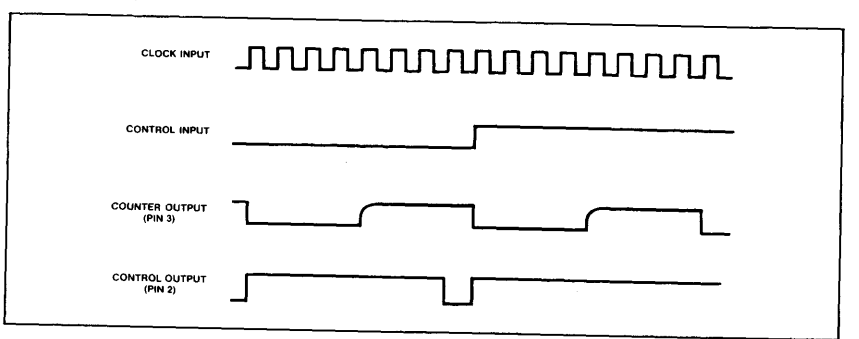


Fig.3 Timing diagram for SP8794

OPERATING NOTES

1. The device will normally be driven by capacitively coupling the clock inputs to the outputs of a 2-modulus divider. See Figs. 4 and 5. The maximum frequency of the device when used as a controller is limited by the internal delays and will not operate above 60MHz. When used as a prescaler the device will operate in excess of 120MHz, the maximum frequency being limited by saturation of the counter output stage.
2. The device is normally driven from the very fast edges of a 2-modulus divider and therefore there is no input slew rate problem.
3. The control input (pin 6) is TTL/CMOS compatible.
4. The counter output (pin 3) interfaces with CMOS/TTL by the addition of a pull-up resistor. For interconnecting to CMOS the output can be connected via a pull-up resistor to a supply which should not exceed 12V.
5. When used as a controller the circuit will self-oscillate in the absence of an input signal. This can be prevented by connecting a 47k resistor from pin 7 to ground, as shown in Fig. 5.
6. The control output which includes an internal 16k pull-down resistor, is ECL compatible and interfaced directly with, for example, the SP8695. See Fig. 5.
7. The propagation delays stated are with a 10k pull-down resistor which is the input pull-down of the SP8695. For interfacing with the SP8643/47 series, which have 4.3k input pull-downs, the propagation delays will be reduced.

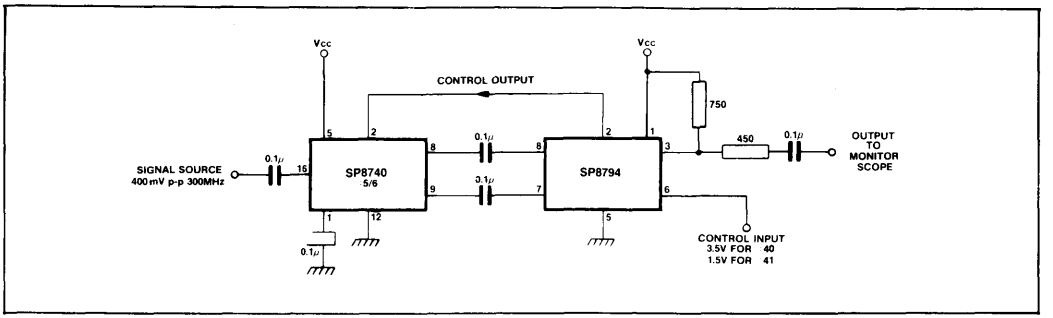


Fig.4 Test circuit

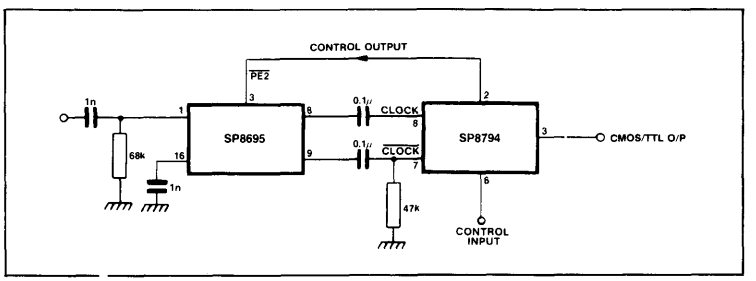


Fig.5 Typical interfacing to suppress self oscillation with no input signal

NJ8820

FREQUENCY SYNTHESISER (PROM INTERFACE)

The NJ8820 is a synthesiser circuit fabricated with the ISO-CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 12-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'N' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words read from an external memory with the necessary timing signals generated internally.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- >10MHz Input Frequency

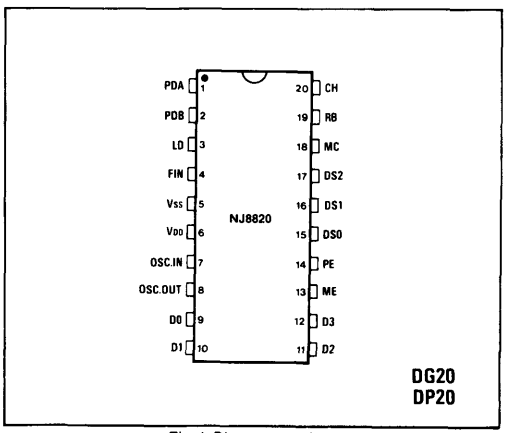


Fig.1 Pin connections

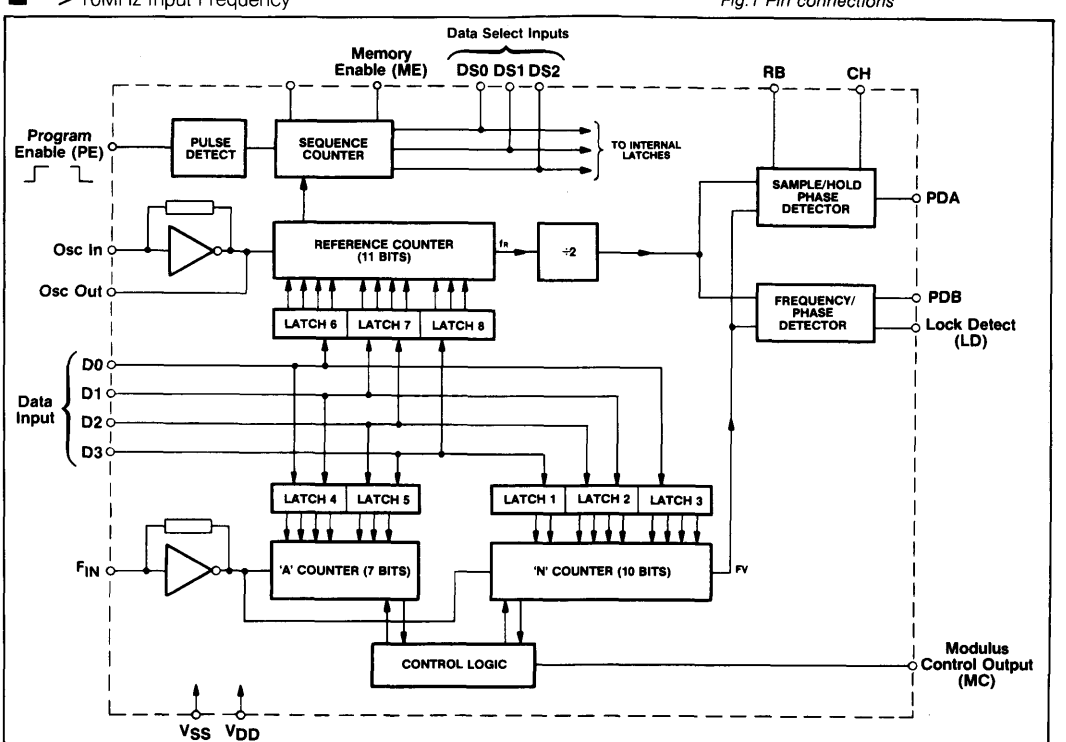


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V Temperature range -30°C to +70°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5	mA	FOSC, FIN = 10MHz } 0 to 5V
		0.7	1	mA	FOSC, FIN = 1.0MHz } square wave
OUTPUT LEVELS					
ME output					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
DS OUTPUTS					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 2mA
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input (PE)					
Trigger level	V_{bias} ±100mV			V	V_{bias} = self bias point of PE (nominally V_{DD}/2)

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS} Note 5
Propagation delay, clock to modulus control		30	50	ns	Note 2
Program enable pulse length, t_W	5			μs	Pulse to V_{SS} or V_{DD}
Data set-up time, t_{SI}	1			μs	
Data hold time, t_{HI}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	
Power supply rise time	100			μs	10 % to 90 %. Note 4

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5us.
4. To ensure correct operation of power-on programming.
5. Opertion at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analogue output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The programme range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10, 11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
13	ME	An open-drain output for use in controlling the power supply to an external ROM or PROM. This output is low during the data read period and high impedance at other times.
14	PE	A positive or negative pulse or edge AC coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner.
15,16,17	DS0-DS2	Internally generated three-state data-select outputs which may be used to address external memory.
18	MC	Signal for controlling an external dual modulus pre-scaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'N' counter completes its cycle at which point both counters are reset. This gives a total division ratio of N.P +A where P and P +1 represent the dual modulus prescale values. The programme range of the 'A' counter is 0-127 and therefore can control pre-scalers with a division ratio up to and including ÷128/129. The programme range of the 'N' counter is 3-1023 and for correct programme operation N ⩾ A. Where every possible channel is required, the minimum division ratio should be P^2-P.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}): -0.5V to 10V
Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature: -65° C to +150° C (DG Package)
Storage temperature: -55° C to +125° C (DP Package)

*Except on open drain outputs where this is 10V.

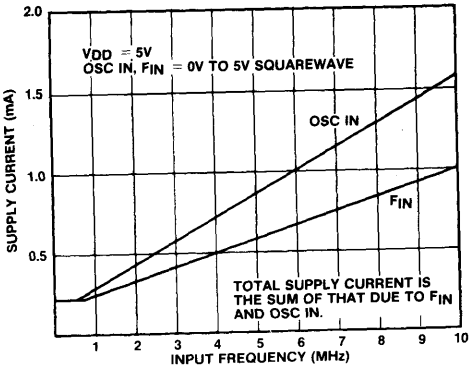


Fig.3 Typical supply current versus input frequency

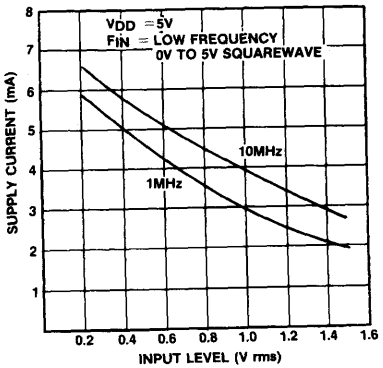


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Program information can be obtained from an external ROM or PROM under control of the NJ8820. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data-transfer time slot and may be used for external control purposes. A suitable PROM may be the 74S287 giving up to 32 channel capability as shown in Fig.3. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25μs.

Reading of this data is normally done in a single shot mode with the data read cycle started by either a positive or negative pulse on the program enable pin. The data read cycle is generated from a program clock at 1/64th of the reference oscillator frequency. A memory enable signal is supplied to allow power-down of the memory when not in use. Data select outputs remain in a high-impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired. The data read cycle, data map and timing diagram appears as Figs.6 to 8. Data is latched internally during the shaded portions of the program cycle and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded causing the data read cycle to repeat in a cyclic manner to allow continuous up-dating of the program information. In this mode external memory will be enabled continuously, (ME low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every 1024/fosc seconds. This programming method is not recommended because the higher power consumption and the possibilities of noise injection into the loop from the digital data lines.

Power-on programming On power-up the data read cycle is automatically initiated making it unnecessary to provide a PE pulse on power-up. The circuit detects the power supply rising above a threshold point, (nominally 1.5V) and after an internally generated delay to allow the supply to rise fully the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function the power supply rise time should be less than 5ms, (at 10MHz) rising smoothly through the threshold point.

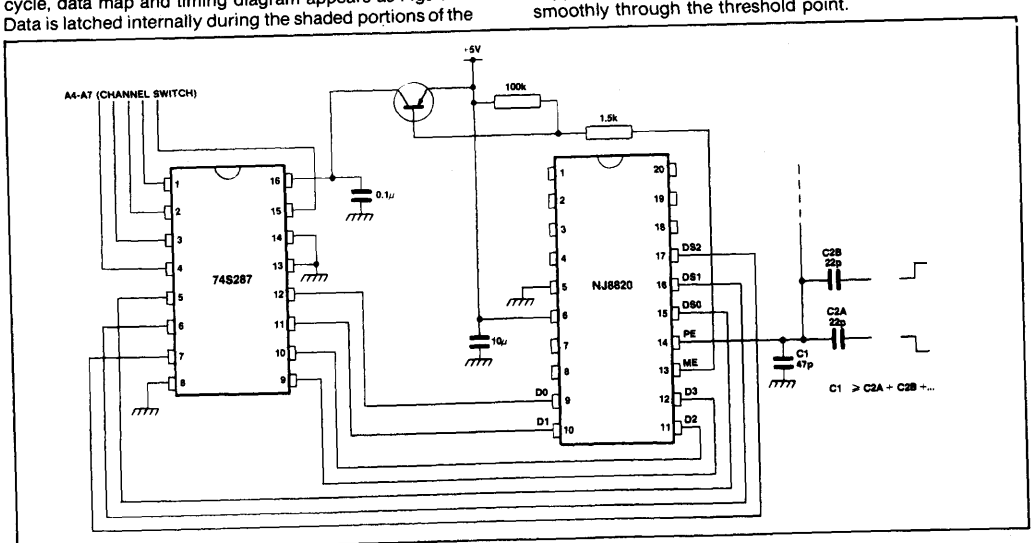


Fig.5 Programming via PROM

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	N1	N0	-	-
2	0	0	1	N5	N4	N3	N2
3	0	1	0	N9	N8	N7	N6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.6 Data map

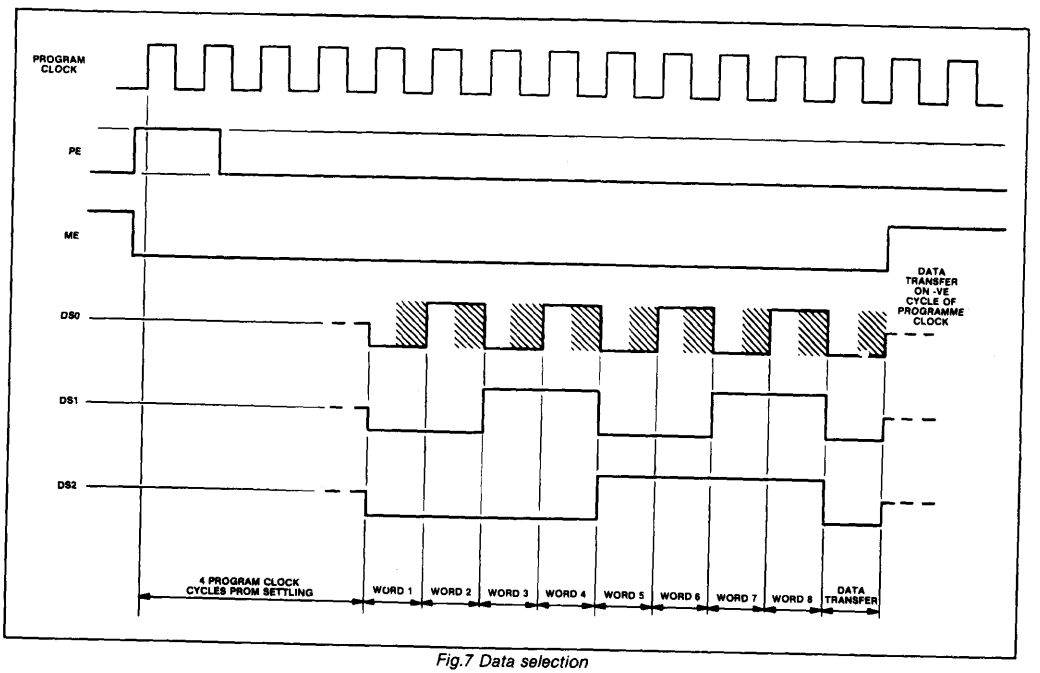


Fig.7 Data selection

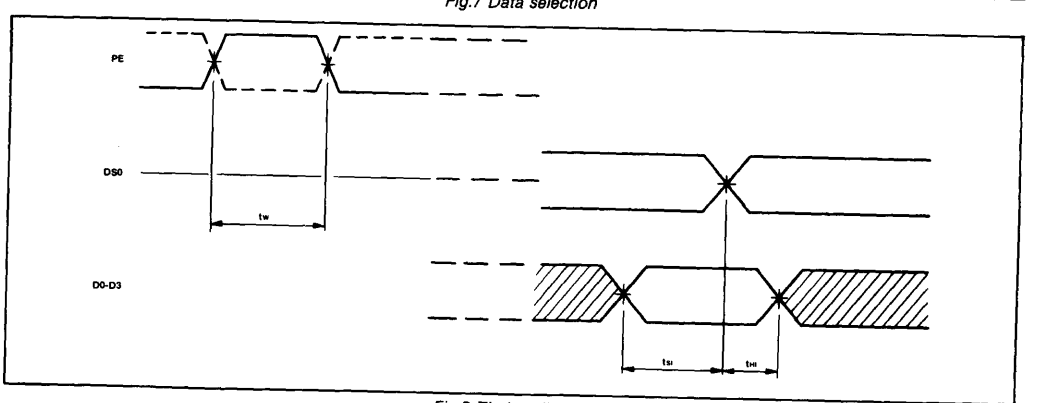


Fig.8 Timing diagram

PHASE COMPARATORS

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

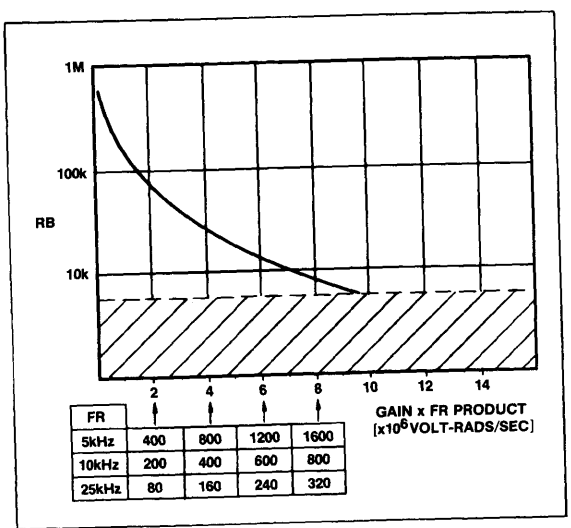
An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-½})]}{2 \times \pi \times 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.9 for example shows that to achieve a gain of 380V per radian at 10kHz requires 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.9 shows the gain normalised to a 1Hz comparison frequency; to obtain the value for any other frequency, divide the value of gain frequency product by the desired frequency.

The output from these phase detectors should be combined and filtered to generate a single control voltage to drive the VCO as in Fig.8.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.9 RB versus gain and reference frequency

APPLICATION EXAMPLE

An application example for a synthesiser for operation up to 520MHz is given in Fig.10. This gives up to 32 channels with a maximum supply current of 17mA, (typically 12mA) at 520MHz excluding the VCO. With careful construction the circuit is capable of providing sideband attenuation in excess of 90dB with lock-times of only a few milliseconds for a 1MHz frequency step.

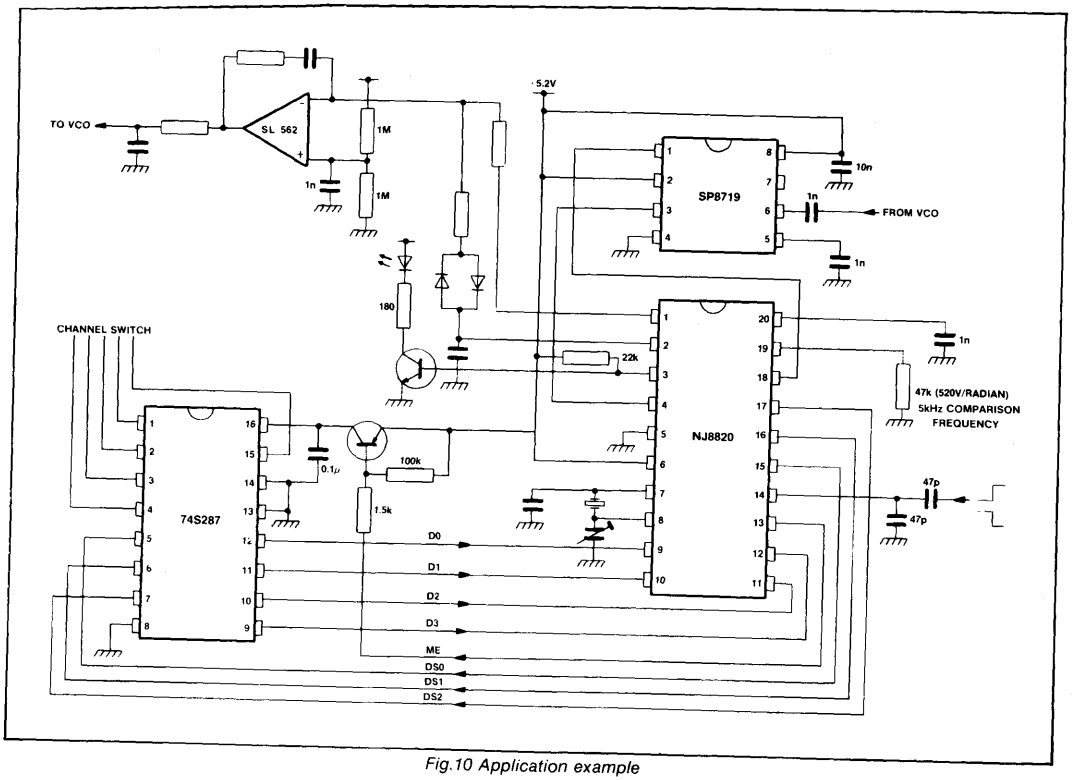


Fig.10 Application example

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NJ8820HG/EXP

HIGH PERFORMANCE FREQUENCY SYNTHESISER

The NJ8820HG is a synthesiser circuit fabricated with the ISO-CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 12-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'N' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words in one of two modes. Data may be read from an external memory with the necessary timing signals generated internally or under external control from a suitable microprocessor. Thus it incorporates the programming features of both the NJ8820 and NJ8821.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

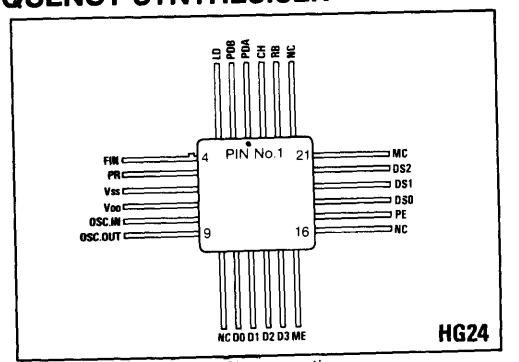


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- Direct Interface to ROM or PROM
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- >10MHz Input Frequency

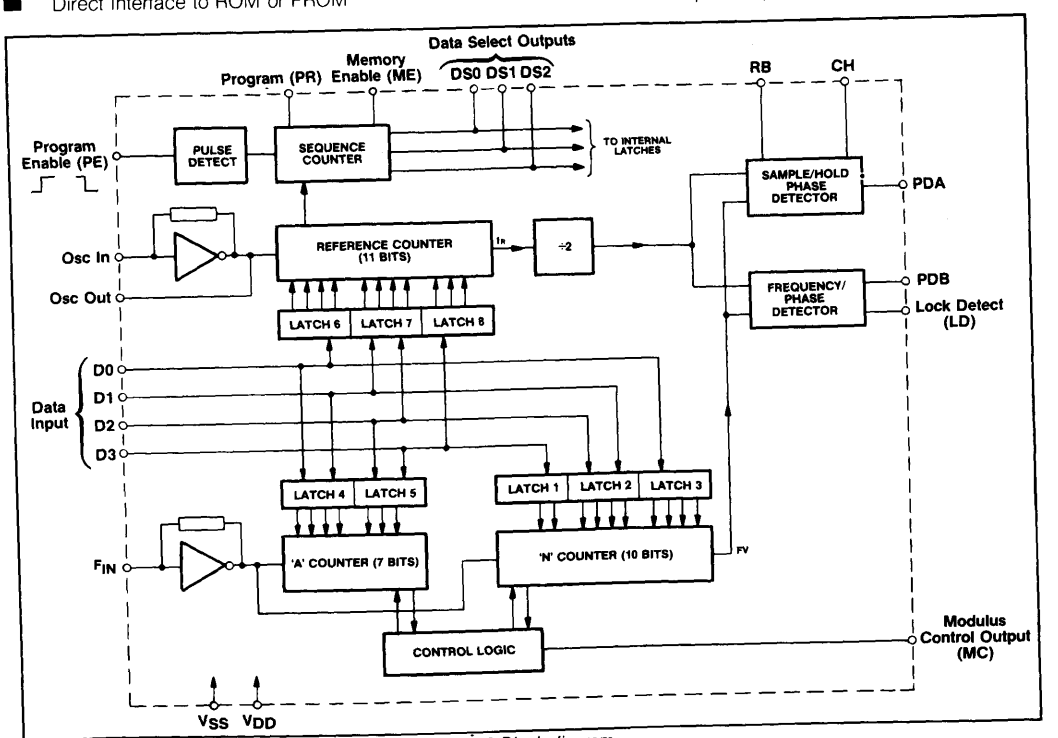


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V Temperature range -30° C to +70° C

DC Characteristics at V_{DD} = 5V

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
Supply current		3.5	5	mA	FOSC, FIN = 10MHz } 0 to 5V
		0.7	1	mA	FOSC, FIN = 1.0MHz } square wave
OUTPUT LEVELS					
ME output					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
DS OUTPUTS					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 2mA
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input (PE)					
Trigger level	V_{bias} ±100mV			V	V_{bias} = self bias point of PE (nominally V_{DD}/2)

AC Characteristics

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS} Note 5
Propagation delay, clock to modulus control		30	50	ns	Note 2
Program enable pulse length, t_w	5			μs	Pulse to V_{SS} or V_{DD}
Data set-up time, t_{SI}	1			μs	
Data hold time, t_{HI}	10			ns	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.7
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	
Power supply rise time	100			μs	10 % to 90 %. Note 4

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5us.
4. To ensure correct operation of power-on programming.
5. Operation at up to 15MHz is possible with a full logic swing but is not guaranteed.

PIN DESIGNATION

Pin No.	Name	Description
1	PDA	Analogue output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	PR	This pin exists only on the flatpack version and allows selection between programming modes. For internal control the pin should be left open circuit and should be grounded to allow external control.
6	V_{SS}	Negative supply (normally ground)
7	V_{DD}	Positive supply
8,9	OSC.IN OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The programme range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
11,12, 13,14	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
15	ME	An open-drain output for use in controlling the power supply to an external ROM or PROM. This output is low during the data read period and high impedance at other times.
17	PE	This pin has two functions. In internal mode a positive or negative pulse or edge AC coupled into this pin initiates the single-shot data read procedure. Grounding this pin repeats the data read procedure in a cyclic manner. In external mode this pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
18,19,20	DS0-DS2	Internally generated three-state data-select outputs which may be used to address external memory. In external mode these pins became inputs to control the addressing of data latches.
21	MC	Signal for controlling an external dual modulus pre-scaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'N' counter completes its cycle at which point both counters are reset. This gives a total division ratio of N.P +A where P and P +1 represent the dual modulus prescale values. The programme range of the 'A' counter is 0-127 and therefore can control pre-scalers with a division ratio up to and including ÷128/129. The programme range of the 'N' counter is 3-1023 and for correct programme operation N ⩾A. Where every possible channel is required, the minimum division ratio should be P^2-P.
23	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
24	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}): -0.5V to 10V
Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V

Storage temperature: -65°C to +150°C

*Except on open drain outputs where this is 10V.

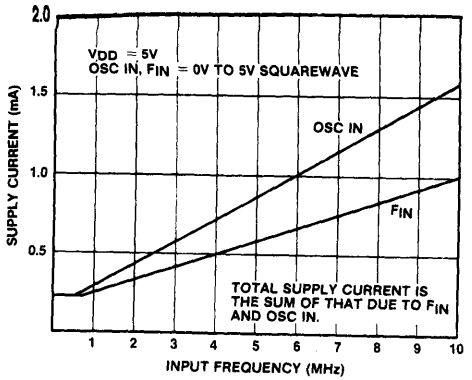


Fig.3 Typical supply current versus input frequency

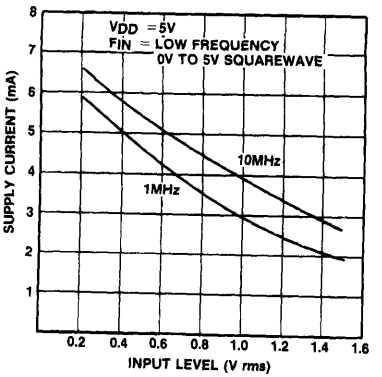


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING IN INTERNAL MODE

This mode of operation allows program information to be obtained from an external ROM or PROM under control of the NJ8820HG. Twenty-eight data bits are required per channel arranged as eight 4-bit words leaving four redundant bits, two of which are available on the data bus driving the data-transfer time slot and may be used for external control purposes. A suitable PROM may be the 74S287 giving up to 32 channel capability. Note that the choice of PNP transistor and supply bypass capacitor on the ROM should be such that the ROM will power up in time: for example, at 10MHz oscillator frequency, the ROM must be powered up in less than 25μs.

Reading of this data is normally done in a single shot mode with the data read cycle started by either a positive or negative pulse on the program enable pin. The data read cycle is generated from a program clock at 1/64th of the reference oscillator frequency. A memory enable signal is supplied to allow power-down of the memory when not in use. Data select outputs remain in a high-impedance state when the program cycle is completed to allow the address bus to be used for other functions if desired.

Data is latched internally during the shaded portions of the program cycle and all data is transferred to the counters and latched during the data transfer time slot.

Alternatively, the PE pin may be grounded causing the data read cycle to repeat in a cyclic manner to allow continuous up-dating of the program information. In this mode external memory will be enabled continuously, (ME low) and the data read cycle will repeat every sixteen cycles of the internal program clock, i.e. every 1024/fosc seconds.

This programming method is not recommended because of higher power consumption and the possibilities of noise injection into the loop from the digital data lines.

Power-on programming On power-up the data read cycle is automatically initiated making it unnecessary to provide a PE pulse on power-up. The circuit detects the power supply rising above a threshold point, (nominally 1.5V) and after an internally generated delay to allow the supply to rise fully the circuit is programmed in the normal way. This delay is generated by counting reference oscillator pulses and is therefore dependent on the crystal used. The delay consists of 53248 reference oscillator cycles giving a delay of about 5ms at 10MHz.

To ensure correct operation of this function the power supply rise time should be less than 5ms, (at 10MHz) rising smoothly through the threshold point.

PROGRAMMING IN EXTERNAL MODE

The external mode of programming is selected by grounding the program pin, (PR). In this mode timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is again as Fig.6 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.8.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	N1	N0	-	-
2	0	0	1	N5	N4	N3	N2
3	0	1	0	N9	N8	N7	N6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

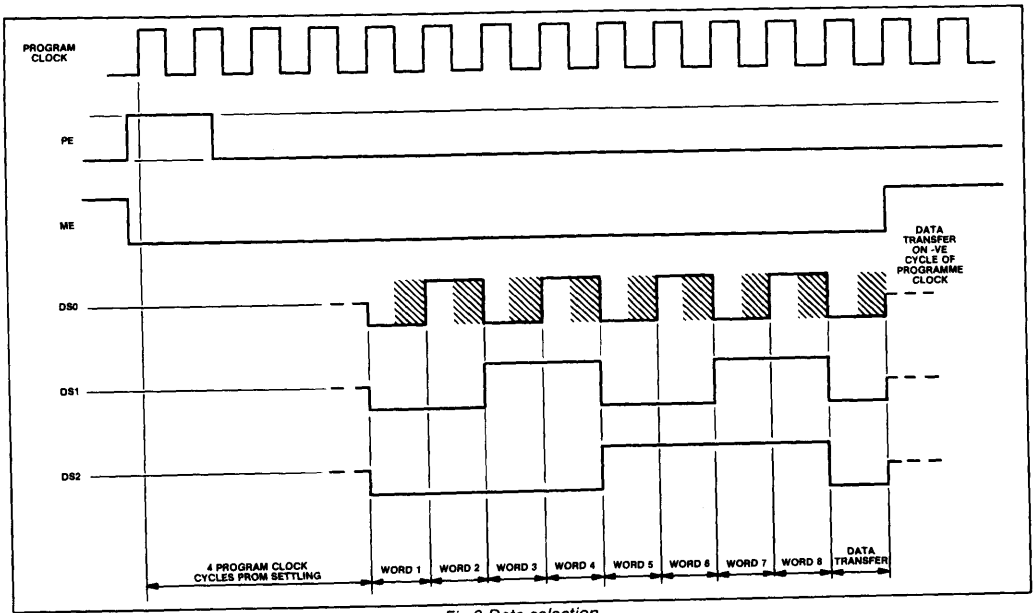


Fig.6 Data selection

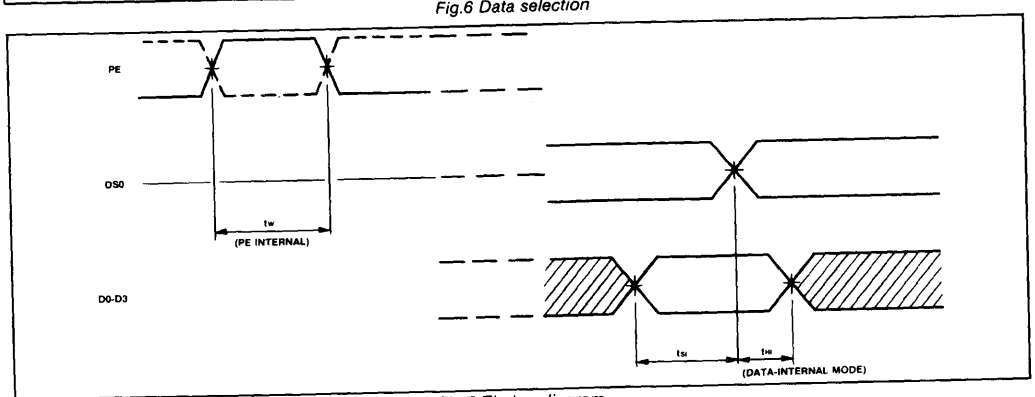


Fig.7 Timing diagram

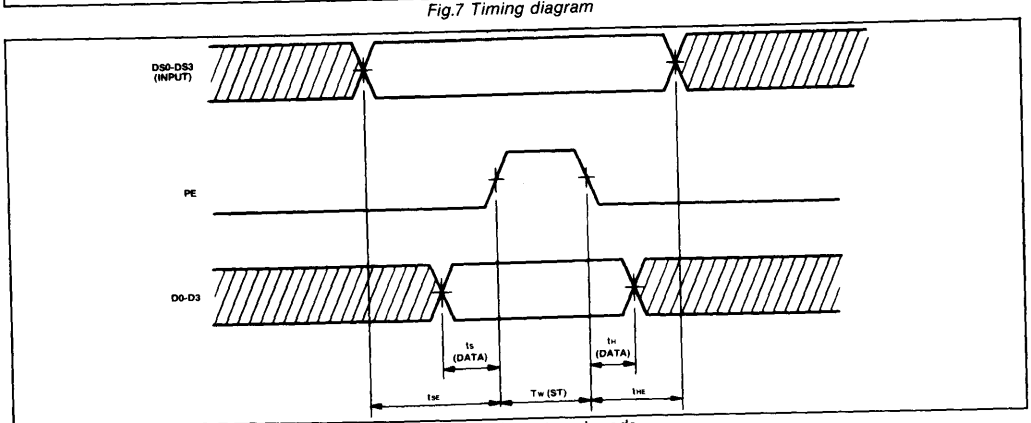


Fig.8 Timing for external mode

PHASE COMPARATORS

A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at $(V_{DD}-V_{SS})/2$ and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}-V_{SS}-0.7-89(RB^{-\frac{1}{2}})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

The value of RB should be chosen to give the required gain at the reference frequency used. Fig.9 for example shows that to achieve a gain of 380V per radian at 10kHz requires 32kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.9 shows the gain normalised to a 1Hz comparison frequency: to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.

FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

Fig.9 RB versus gain and reference frequency

PLESSEY
Semiconductors

NJ8821

FREQUENCY SYNTHESISER (MICROPROCESSOR INTERFACE)

The NJ8821 is a synthesiser circuit fabricated with the ISO-CMOS process and is capable of achieving high sideband attenuation and low noise performance. The circuit contains a reference oscillator, 12-bit programmable reference divider, digital and sample-and-hold phase comparators, 10-bit programmable 'N' counter, 7-bit programmable 'A' counter and the necessary control and latch circuitry for accepting and latching the input data.

Data is presented as eight 4-bit words under external control from a suitable microprocessor.

It is intended to be used in conjunction with a two-modulus prescaler such as the SP8710 series to produce a universal binary coded synthesiser.

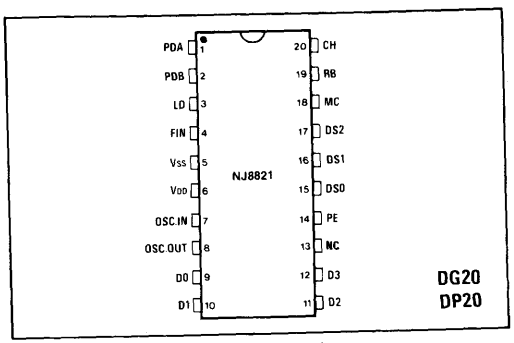


Fig.1 Pin connections

FEATURES

- Low Power Consumption
- High Performance Sample and Hold Phase Detector
- Microprocessor Compatible
- >10MHz Input Frequency

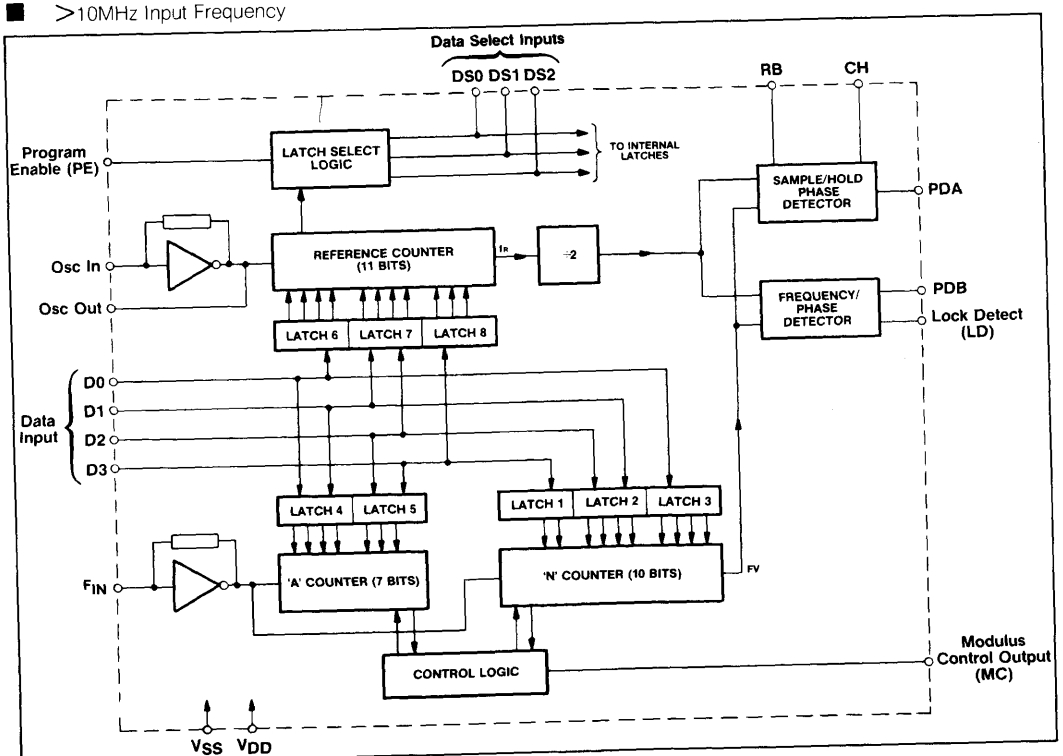


Fig.2 Block diagram

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
V_{DD}-V_{SS} 5V ± 0.5V
Temperature range -30°C to +70°C

DC Characteristics at V_{DD} = 5V

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
Supply current		3.5	5	mA	FOSC, FIN = 10MHz, 0 to 5V
		0.7	1	mA	FOSC, FIN = 1.0MHz, square wave
MODULUS CONTROL OUT					
High level	4.6			V	I_{source} 1mA
Low level			0.4	V	I_{sink} 1mA
LOCK DETECT OUT					
Low level			0.4	V	I_{sink} 4mA
Open drain pull-up voltage			8	V	
PDB Output					
High level	4.6			V	I_{source} 5mA
Low level			0.4	V	I_{sink} 5mA
3-state leakage			±0.1	μA	
INPUT LEVELS					
Data Inputs					
High level	4.25			V	TTL compatible
Low level			0.75	V	See note 1
Program Enable Input					
High level	4.25			V	
Low level			0.75	V	
DS INPUTS					
High level	4.25			V	
Low level			0.75	V	

AC Characteristics

Characteristics	Value			Units	Conditions
	Min.	Typ.	Max.		
FIN/OSC inputs	200			mV RMS	10MHz AC coupled sinewave
Max. operating freq. OSC/FIN inputs	10.6			MHz	V_{DD} = 5V, Input squarewave V_{DD}-V_{SS}. Note 4
Propagation delay, clock to modulus control		30	50	ns	Note 2
Strobe pulse width external mode, $t_{w(ST)}$	2			μs	
Data set-up time, $t_{s(DATA)}$	1			μs	
Data hold time, $t_{H(DATA)}$	1			μs	
Address set-up time, t_{SE}	1			μs	
Address hold time, t_{HE}	1			μs	
Digital phase detector propagation delay		500		ns	
Gain programming resistor, RB	5			kΩ	See Fig.6
Hold capacitor, CH			1	nF	Note 3
Output resistance PDA			5	kΩ	
Digital phase detector gain		1		V/Rad	

NOTES
1. Data inputs have internal 'pull-up' resistors to enable them to be driven from TTL outputs.
2. All counters have outputs directly synchronous with their respective clock rising edges.
3. Finite output resistance of internal voltage follower and 'on' resistance of sample switch driving this pin will add a finite time-constant to the loop. A 1nF hold capacitor will give a maximum time-constant of 5μs.
4. Operation at up to 15MHz is likely with a full logic swing but is not guaranteed.

Pin No.	Name	Description
1	PDA	Analogue output from the sample and hold phase comparator for use as a 'fine' error signal. Output at (V_{DD}-V_{SS})/2 when in lock. Voltage increases as FV phase lead increases and decreases as FR phase lead increases. Output is linear over only a narrow phase window determined by gain programmed by RB.
2	PDB	Three-state output from the phase/frequency detector for use as a 'coarse' error signal. FV > FR or FV leading: positive pulses FV < FR or FR leading: negative pulses FV = FR and phase error within PDA window: high impedance
3	LD	An open drain lock detect output at low level when phase error within PDA window (in lock). High impedance at all other times.
4	FIN	The input to the main counters normally driven from a prescaler which may be AC coupled or when a full logic swing is available may be DC coupled.
5	V_{SS}	Negative supply (normally ground)
6	V_{DD}	Positive supply
7,8	OSC.IN OSC.OUT	These pins form an on-chip reference oscillator when a parallel resonant crystal is connected across them. Capacitors of an appropriate value are also required between each end of the crystal and ground to provide the necessary additional phase shift. An external crystal generated reference signal may alternatively be applied to OSC.IN. This may be a low-level signal AC coupled into OSC.IN or if a full logic swing is available it may be DC coupled. The programme range of the reference counter is 6-4094 in steps of 2, with the division ratio being twice the programmed number.
9,10, 11,12	D0-D3	Information on these inputs is transferred to the internal latches during the appropriate data read time slot. D3 MSB, D0 LSB.
14	PE	This pin is used as a strobe for the data. A logic high on this pin transfers data from the data pins to the internal latch selected by the address, (data select) lines, while a logic zero disables the data lines.
15,16,17	DS0-DS2	Data-select inputs to control the addressing of data latches.
18	MC	Signal for controlling an external dual modulus pre-scaler. The modulus control level will be low at the beginning of a count cycle and will remain low until the 'A' counter completes its cycle. The modulus control then goes high and remains high until the 'N' counter completes its cycle at which point both counters are reset. This gives a total division ratio of N.P +A where P and P +1 represent the dual modulus prescale values. The programme range of the 'A' counter is 0-127 and therefore can control pre-scalers with a division ratio up to and including ÷128/129. The programme range of the 'N' counter is 3-1023 and for correct programme operation N ≥A. Where every possible channel is required, the minimum division ratio should be P^2-P.
19	RB	An external sample and hold phase comparator gain programming resistor should be connected between this pin and V_{SS}.
20	CH	An external hold capacitor should be connected between this pin and V_{SS}.

ABSOLUTE MAXIMUM RATINGS

Supply voltage (V_{DD}-V_{SS}): -0.5V to 10V
Input voltage at any pin * V_{SS} -0.3V to V_{DD} +0.3V
Storage temperature: -65° C to +150° C (DG Package)
Storage temperature: -55° C to +125° C (DP Package)

*Except on open drain outputs where this is 10V.

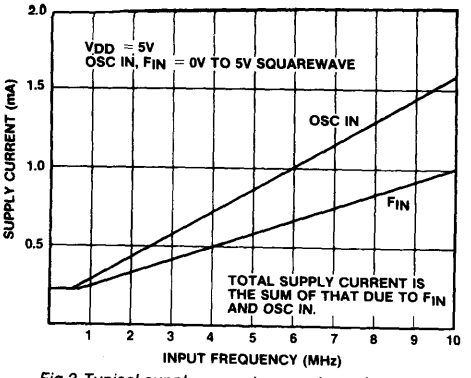


Fig.3 Typical supply current versus input frequency

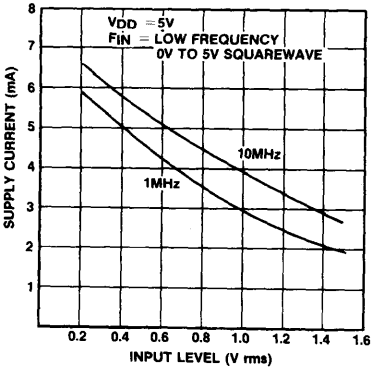


Fig.4 Typical supply current versus input level, Osc In

PROGRAMMING

Timing is generated externally, normally from a microprocessor, and allows the user to change the data in selected latches. The data map is Fig.3 with the PE pin used as a strobe for the data. Taking the PE pin high will transfer data from the data pins into the selected latch and taking this pin low will disable the data pins, retaining that data on the selected latch. Data transfer from all internal latches into the counters will occur simultaneously with the transfer of data into latch 1 and therefore this would normally be the final latch addressed during each channel change. Timing information for this mode of operation is given in Fig.6.

WORD	DS2	DS1	DS0	D3	D2	D1	D0
1	0	0	0	N1	N0	-	-
2	0	0	1	N5	N4	N3	N2
3	0	1	0	N9	N8	N7	N6
4	0	1	1	A3	A2	A1	A0
5	1	0	0	-	A6	A5	A4
6	1	0	1	R3	R2	R1	R0
7	1	1	0	R7	R6	R5	R4
8	1	1	1	-	R10	R9	R8

Fig.5 Data map

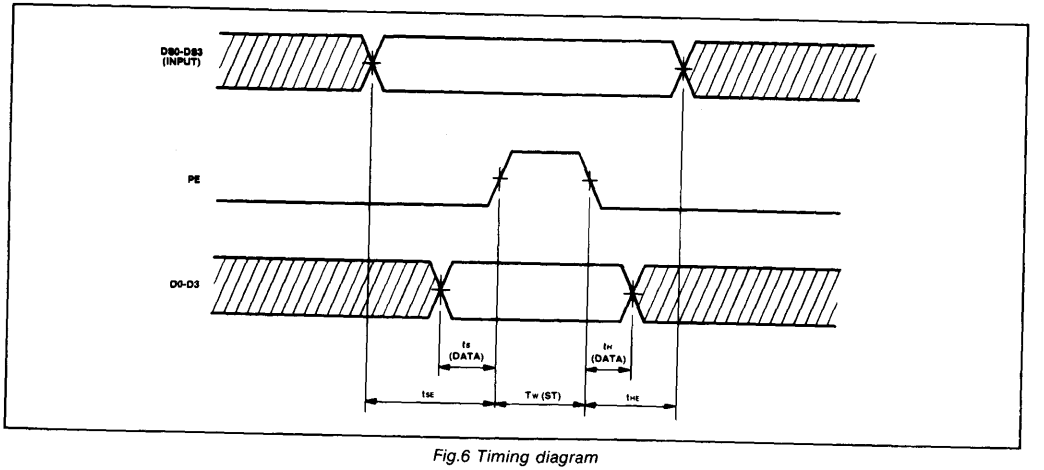


Fig.6 Timing diagram

PHASE COMPARATORS

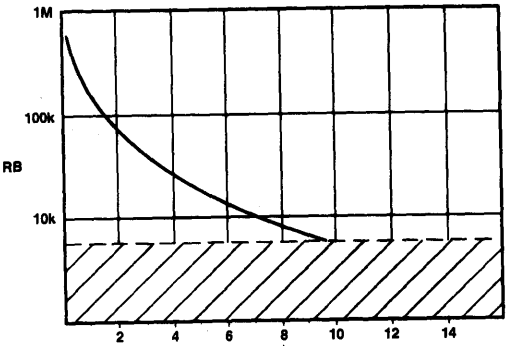
A standard digital phase/frequency detector driving a three-state output provides a 'coarse' error signal to enable fast switching between channels. This output is active until the phase error is within the sample and hold phase detector window, when its output becomes high impedance. Phase-lock is indicated at this point with a low level on LD. The sample and hold phase detector provides a 'fine' error signal to give further phase adjustment and to hold the loop in lock.

An internally generated ramp controlled by the digital output from both the reference and main divider chains is sampled at the reference frequency to give the fine error signal, PDA. When in phase lock this output would typically be at (V_{DD}-V_{SS})/2 and any offset from this would be proportional to phase error. The relationship between this offset voltage and the phase error is the phase-comparator gain which is programmable with an external resistor, RB. An internal 50pF capacitor is used in the sample and hold comparator.

This gain is typically:

$$\text{GAIN} = \frac{10\,[V_{DD}\text{-}V_{SS}\text{-}0.7\text{-}39(RB^{-\frac{1}{2}})]}{2 \times \pi\ 50\times10^{-12} \times RB \times FR}$$

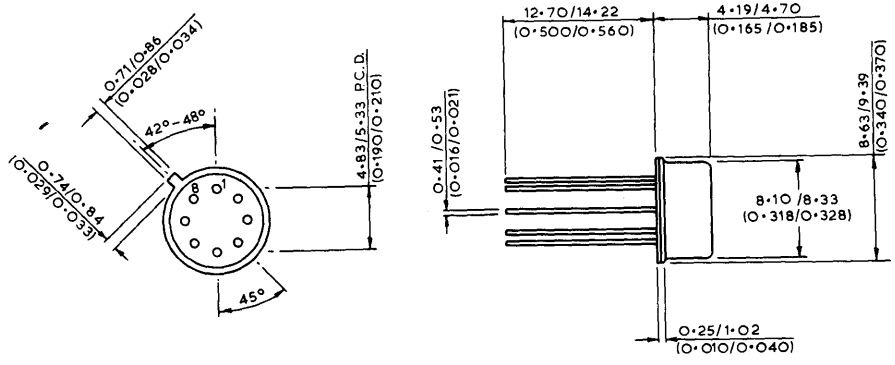
The value of RB should be chosen to give the required gain at the reference frequency used. Fig.7 for example shows that to achieve a gain of 380V per radian at 10kHz requires 39kΩ. A second external component is required; this is a hold capacitor of non-critical value which might typically be 470pF, a smaller value being sufficient if the sideband performance required is not high. Fig.7 shows the gain normalised to a 1Hz comparison frequency: to obtain the value for any other frequency, divide the value of Gain Frequency product by the desired frequency.



FR				
5kHz	400	800	1200	1600
10kHz	200	400	600	800
25kHz	80	160	240	320

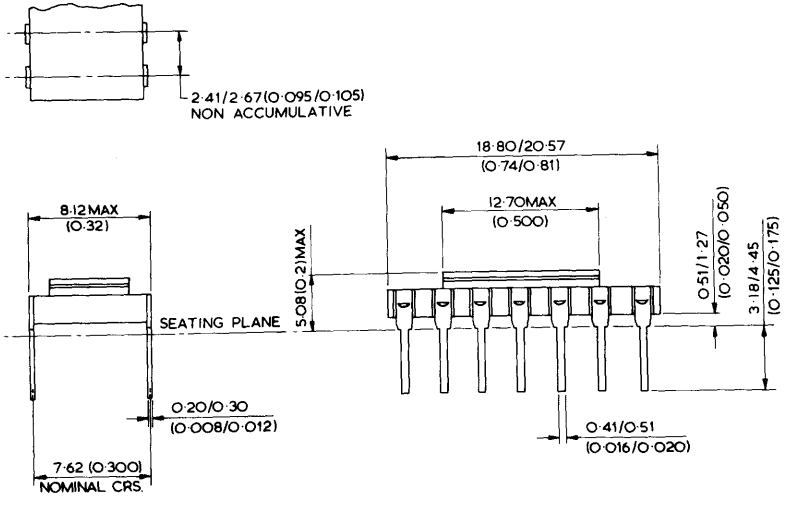
Fig.7 RB versus gain and reference frequency

Package Outlines



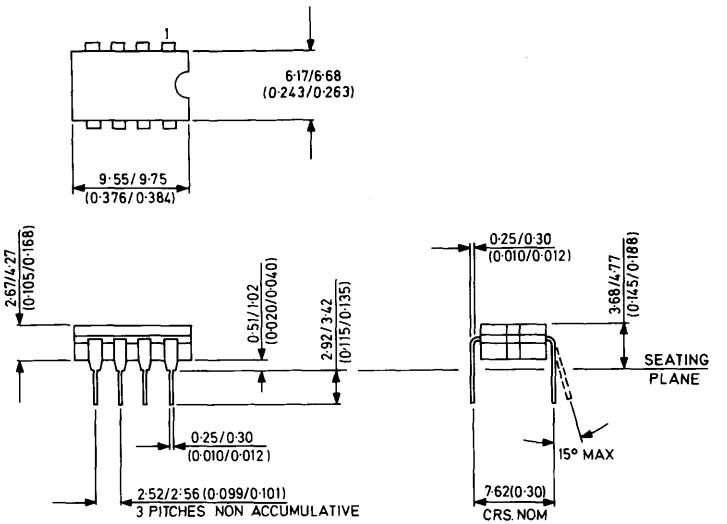
8 LEAD TO8

CM8



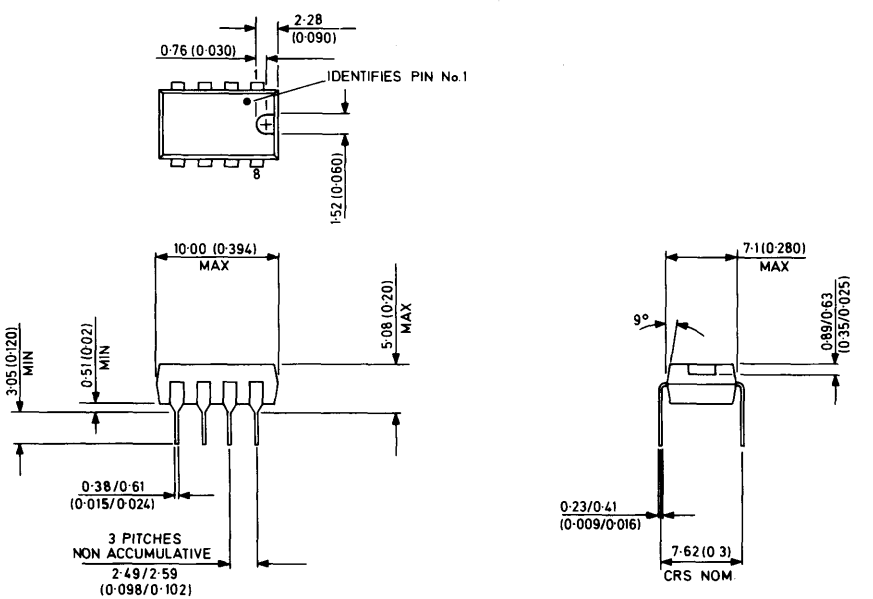
14 LEAD DILMON

DC14



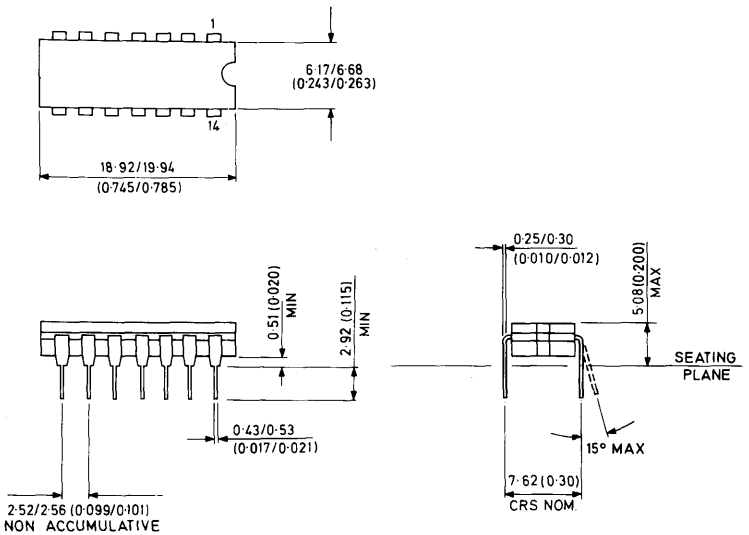
8 LEAD CERAMIC DIL

DG 8



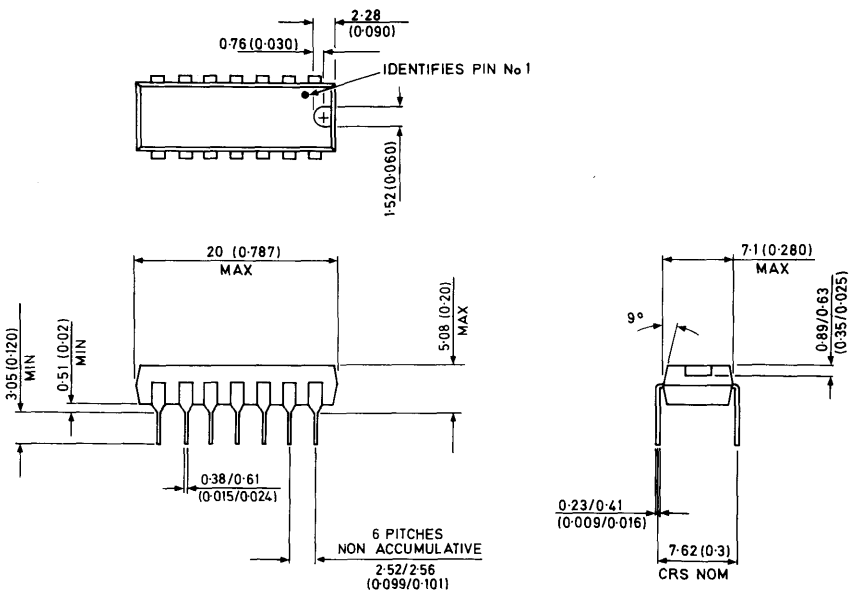
8 LEAD PLASTIC DIL

DP 8



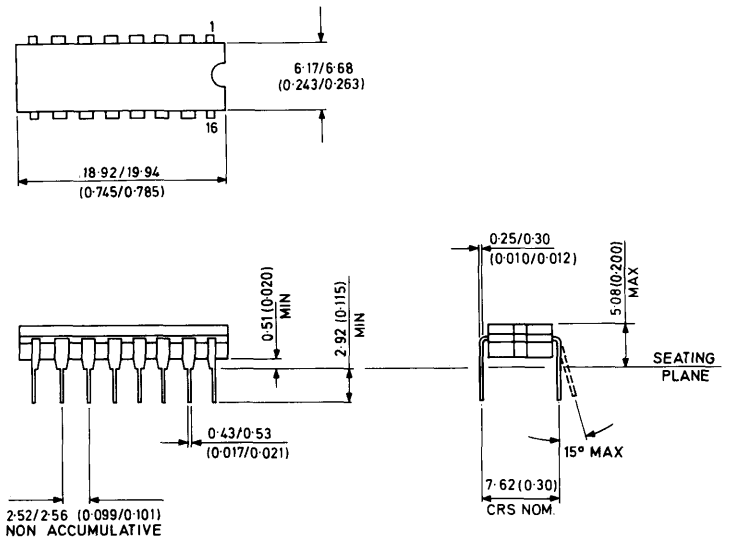
14 LEAD CERAMIC DIL

DG14



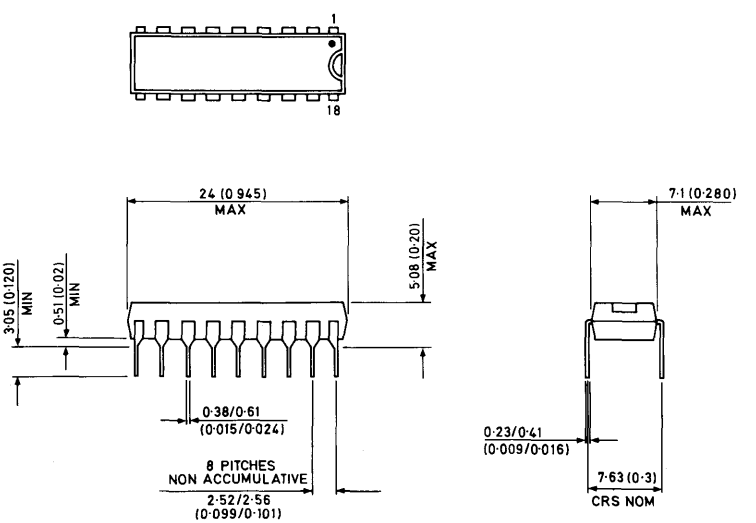
14 LEAD PLASTIC DIL

DP14



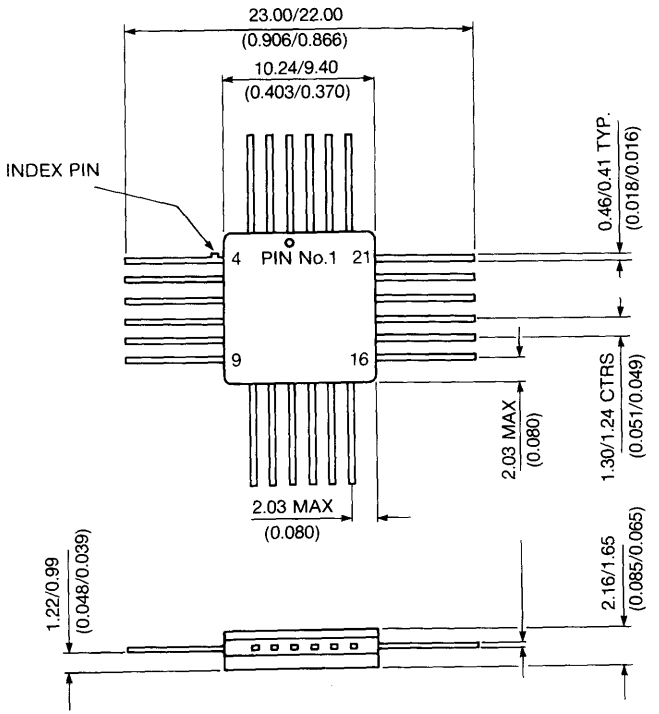
16 LEAD CERAMIC DIL

DG16



18 LEAD PLASTIC DIL

DP18



24 LEAD FLATPACK

HG24

Packaging and ordering information

Plessey Semiconductors integrated circuits are allocated type numbers which take the following general form

WW XXXX Y/ZZ

where **WW** is a two-letter code identifying the product group and/or technology, **XXXX** is a three or four numeral code uniquely specifying the particular device, **Y** is a single letter which denotes the precise electrical or thermal specification for certain devices and **ZZ** is a two-letter code defining the package style. Digits **WW**, **XXXX** and **Y** must always be used when ordering; digits **ZZ** need only be used where a device is offered in more than one package style. For example, the **NJ8820** is offered in **DG** (Ceramic dual-in-line) and **DP** (Plastic dual-in-line) packages so the full ordering number for this device in ceramic DIL would be **NJ8820/DG.**

The Pro-Electron standard is used for package codes wherever possible. The two letters of this code have the following meanings:

FIRST LETTER (indicates general shape)

A Pin-Grid Array
C Cylindrical
D Dual-in-Line (DIL)
F Flat Pack (leads on two sides)
G Flat Pack (leads on four sides)
Q Quad-in-Line

M Miniature (for Small Outline)
L Leadless Chip Carrier
H Leaded Chip Carrier

Not yet designated by Pro-Electron

SECOND LETTER (indicates material)

C Metal-Ceramic (Metal Sealed)
G Glass-Ceramic (Glass Sealed)
M Metal
P Plastic
E Epoxy

Note: Gull-winged Quad Cerpac is a Flat Pack with leads on 4 sides hence it will be represented by GG.

Please Note:

Leadless Chip Carriers

LC Metal-Ceramic 3 Layer (Metal Sealed)
LG Glass-Sealed Ceramic
LE Epoxy-Sealed 1 Layer
LP Plastic

Packaging and ordering information (cont.)

Leaded Chip Carriers

Where supplied without lead forming, flat pack rules apply. Where leads are bent under to form footprints equivalent to leadless chip carriers then use H.

e.g. **HG** Glass-Sealed Ceramic Leaded Chip Carrier (J Leaded Quad Cerpac)
HP Plastic Leaded Chip Carrier

Note: The above information refers generally to all Plessey Semiconductors integrated circuit products and does not necessarily apply to devices contained in this handbook.

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